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Air cooling of a microelectronic chip with diverging metal microchannels monolithically processed using a single mask

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Abstract

A single-mask process is used to fabricate metal microchannels of $5-10 \mu$ m in width, 10–40 μ m in height and millimeters in length, monolithically (i.e., no bonding) on the chip front side. Taking advantage of the small size and the diverging cross-section allowed for these microchannels, we explore the air cooling of a microelectronic chip, addressing the limitations of the liquid cooling with the well-known silicon bulk-etched microchannels. Upon the air flow, a distributed array of temperature sensors integrated on a heater chip reads a temperature drop (e.g., from 90 °C to 25–27 °C) and confirms an effective cooling. A thermal analysis further predicts a heat removal capacity of more than 35 W cm⁻² by optimized microchannels with a pressure drop of 30 psi (207 kPa). The compatibility with IC fabrication and the use of air as the coolant makes the chip packaging and the system implementation of the reported approach simpler and economical for microelectronic chip cooling.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

1.1. Motivation

With the increase in device density on integrated circuit (IC) chips, heat removal has been an important consideration. Among various cooling schemes proposed to date, heat sinks with microchannels are among the most promising [1]. The first was made of silicon with a channel cross-section on the order of 50 μ m in width and 300 μ m in depth, reporting a heat removal flux as high as 790 W cm⁻² by flowing a cooling liquid through the channels [2]. However, this heat sink suffered from the cost of implementation such as bonding of the heat sink to the chip, modification of the chip packaging procedure and the complexity of the electronic system hosting coolant recirculation, as well as the cost of the silicon microchannel heat sink. To address these problems, we develop a microchannel fabrication method that is of low

cost not only for the formation of the channels but also for the chip packaging. Using only a standard ultraviolet (UV) light source and one photomask minimizes the cost of the channel fabrication. By building metal microchannels of a hydraulic diameter of only 10–30 μ m and allowing a diverging cross-section, we verify that even air can be explored as a cooling medium, which would not call for the complex electronic system that a liquid cooling would.

Over the past 20 years, the construction of miniaturized channels has become increasingly important not only for IC chip cooling but more so in many other applications. A number of micro analysis systems such as gas chromatography, liquid chromatography, free-flow fractionation and electrophoresis have been developed by micromachining technology, requiring such microchannels for reactant delivery and biochemical reaction chambers. Other applications are found in liquid flow sensors, pressure and drag force flow sensor, densitometer, micropumps, micro thermal actuator and in passive liquid flow devices such as micro filters and microvalves [3]. Before describing our microchannels, a review of microchannel fabrication methods to date is presented.

1.2. Review of microchannel fabrication methods

Terry et al [4] fabricated one of the first micromachined channels as a part of a gas chromatography analyzer by isotropic etching grooves into a silicon substrate and bonding a Pyrex glass cover plate on top. Tuckerman and Pease [2] anisotropically etched deep grooves into a (110) silicon chip and formed microchannels by a glass-to-silicon direct bonding for IC chip cooling. Weber [5] has developed a method to build microchannels directly on the top surface of IC chips, eliminating the need for bonding. Thin metallic or plastic tubes were placed on the surface as mold to form microchannels by electroplating. However, since the molding material had to be etched away from the ends of the channel, the obtainable length of the channels was limited in practice. More importantly, this method could not be incorporated into standard IC processing. These limitations prompted us to develop a fabrication method reported in this paper. Shoji et al [6] developed a fabrication process that used positive photoresist (PR) as a sacrificial layer and negative PR as a structure layer yielding 1–5 μ m high channels. However, the size of the microchannels was limited by the height of the sacrificial layer. Kaplan et al [7] proposed microchannels made by undercut etching into quartz wafer through a polysilicon mask layer and sealing the openings by thermal oxidation or low-pressure chemical vapor deposition (LPCVD) oxide deposition. Schomburg et al [8] made microchannels for a microvalve device using the LIGA technique, plastic molding and polymer bonding. Mallik et al [9] made triangular cross-section microchannels for micro heat pipe arrays after first forming anisotropically etched grooves and eventually closing the grooves with a metal layer by a dual electron beam vapor deposition. Joo et al [10] introduced a one-mask process to fabricate a long metallic microchannel, serving as the basis for those reported in this paper.

Chen and Wise [11] proposed a way to fabricate nozzles for inkjet printing. The nozzles were anisotropically etched to undercut a network of highly boron-doped silicon support ribs, forming an array of microchannels which were then sealed using thermal oxidation and LPCVD dielectrics. Enoksson et al [12] made hexagonal cross-section microchannels for the densitometer using double-side anisotropic etching and silicon direct bonding. A compensation layout was proposed to protect the convex corners. Tjerkstra *et al* [13] presented various etching techniques to fabricate channels buried underneath the wafer surface. Utilizing reactive ion etching (RIE), potassium hydroxide (KOH) wet etching and deposition of silicon nitride, this method demonstrated even buried channels traversing each other. Papautsky et al [14] presented surface-machined metallic microchannels. The idea was similar to Joo's [10], but the channels were sealed before completely removing the PR mold material, facing the same length limitation as Weber [5]. Man et al [15] proposed a method to form polymer fluid channels for bioanalysis chips. Unlike Shoji [6], they used a thick positive PR and polyimide

to form the microchannels ranging from 0.5 to 100 μ m in height and several centimeters long, utilizing a thin layer of p-xylylene as a biocompatible barrier of solvent between the PR and the polyimide. Guerin et al [16] used a very thick PR (SU-8) to fabricate a high-aspect-ratio microchannels for thermal flow sensors. A pre-formed structure was filled with another material and covered with the second SU-8. The channel was formed by developing the top SU-8 and dissolving the filler. Vieider et al [17] developed a laser chip carrier with V-grooves for an optical fiber alignment and electrodes for the flip-chip mounting of lasers. Sealed V-grooves were fabricated by first etching out deep structures through a perforated silicon nitride membrane in only one etching step and then sealing it with LPCVD. Somewhat similarly, Kaltsas et al [18] proposed a method to fabricate buried microchannels covered with porous silicon. Porous silicon of a specific depth was first created over a predefined area, and then a cavity was formed underneath it by electropolishing. Yao et al [19] proposed a method based on a mismatched combination of resist and exposure wavelength. The channel side walls were formed by exposing a long wavelength UV into a negative PR, and the sealing layer was formed by a short wavelength UV, demonstrating three-dimensional multi-layer microchannels made of a PR material.

There are several issues to be discussed for the microchannel fabrication methods described above. First, the cost of implementation would be high if wafer bonding is necessary in the process, not only for the cost of process but also the material cost of a silicon or Pyrex wafer. In addition, bonding requires a high temperature and high electrical field, which may damage the electronic devices on the wafer. Second, the fabrication methods largely determine the size, shape and material of microchannels and the layout configuration of their arrays. For surface micromachining, the characteristic size of the microchannel is limited to just a few microns. For wet anisotropic bulk micromachining, a high-aspect-ratio cross-section microchannel can be obtained, but the wafer type and channel orientation is severely limited. Dry anisotropic bulk micromachining (e.g., deep RIE) presents great flexibility, but the cost of the process is often a concern. For isotropic bulk etching, the channel size is limited by the adjacent channels. The methods involving etching into the substrate are not ideal for IC cooling because they cannot be applied to the front side of the IC chip. Third, one should not ignore the consequences to the chip packaging and the eventual electronic system after the microchannels are placed on chip by any of the above methods.

1.3. Cooling with microchannels

The boiling convection in microchannels has been studied mainly because it requires less pumping power than a single-phase liquid convection for a given heat sink thermal resistance [20–24]. Kandlikar [25], Bergles *et al* [26], Celata [27], and Lasance and Simons [1] presented good reviews on a two-phase flow heat transfer in microchannels. Bowers and Mudawar studied the boiling convection in microchannels using R-113 as a coolant [20]. They obtained heat fluxes larger

than 200 W cm⁻² coupled with a low flow rate ($<65 \text{ ml min}^{-1}$) and a low pressure drop (<0.35 bar). In comparison, singlephase microchannel heat sinks using water as a coolant would require more than 1 bar of pressure drop to achieve the same amount of heat flux. A prototype of a 1000 W cm⁻² cooling system based on a boiling heat transfer in microchannel heat sinks using a flow rate of 500 ml min⁻¹ has been described in [28].

However, the main difficulty of a two-phase flow microchannel heat exchanger is the flow instability [1, 25, 26]. The microchannels in most of the studies were aligned parallel. The cross-sectional areas were constant along the channel length, but the coolant volume increased as the coolant flew downstream due to the bubble generation, causing an increase of volume flow rate downstream. When small bubbles merged to form larger bubbles, which blocked a microchannel, a flow reversal occurred in that channel because the expanding bubbles pushed the liquid-vapor interface in both upstream and downstream directions. The total flow in the microchannel heat sink became unstable because the coolant preferred to flow in unblocked channels. Another difficulty is that great care has to be given to introduce the flow evenly into each microchannel. Sometimes a complicated branching distributor, which uses cascades of 'tees', or a circular distributor had to be used.

We propose to use the metallic microchannels described in the next section for IC chip cooling. The problem of long channel etching is solved with a timed electroplating and self-sealing method. The one-mask low-temperature fabrication process can be simply added as the last step during IC fabrication, incurring a small increase in the total cost of the chip production. Furthermore, this method offers a much greater freedom in laying out the channel patterns, allowing to leave the wire bonding areas and wafer dicing kerf lines free of the channels, thus helping the subsequent packaging procedures. The freedom in the layout further allows radially oriented channels as well as parallel channels. The cross-sectional area of radially oriented channels increases as the coolant flows downstream and gets heated. For a boiling convection, such diverging microchannels would help accommodate the increase of the volume flow rate caused by the bubble generation. Moreover, the radially oriented channels do not need a complicated branching distributor because all channels are aligned at the same distance from the coolant inlet section.

2. Single-mask fabrication process of monolithic metal microchannels

The main concept of the fabrication process is schematically described in figure 1, featuring a monolithic construction (i.e., no bonding involved) and the use of only one mask (i.e., no alignment between masks needed). A detailed procedure is presented here as one specific process example. To start, a seed layer comprising 50 Å chromium and 1500 Å of nickel was evaporated on a silicon wafer, with the chromium layer promoting the adhesion between the nickel and the silicon substrate. Next, a layer of PR was spun onto the seed layer.



Figure 1. Schematic diagram describing the main fabrication concept: (*a*) pattern thick PR on the seed layer; (*b*) electroplate metal in the PR mold and continue until the metal covers the mold almost completely; (*c*) remove PR through the openings in the metal; (*d*) resume electroplating to close the openings and complete the channel structures. The electrolyte inside the channels is flushed with DI water before the channels are dried.

AZ 4620, a positive PR of high transparency [29], was an initial choice. The PR was then exposed to an UV light and developed with the AZ 400K developer (figure 1(a)). After the PR mold was formed, nickel was electroplated onto the mold openings to build the channel walls in an electrolytic solution composed of nickel sulfamate, nickel bromide, boric acid, stress reducer and anti-pit agent. The nickel sulfamate served as the nickel carrier during electroplating. The nickel bromide helped dissolve the cathode, but it tended to increase stress in the film. The boric acid in the bath served as a pH buffer (limiting the increase of pH). A stress reducer, consisting mainly of saccharin, relieved residual stress in the film when added in a small amount. A large amount would dull the nickel surface, i.e., the finished surface would not be mirrorlike. During the course of electroplating, there was a visible formation of hydrogen bubbles on the sample. The evolution of hydrogen may create small craters on the film by preventing the electrolytic solution from reaching the plating surface. At a low current density, the evolution of hydrogen bubbles was reduced, and the uniformity of the film was improved. An anti-pit agent was also added in a small amount to reduce



Figure 2. SEM pictures of microchannel cross-sections at two different stages of fabrication: (*a*) incomplete channels with overhangs about to merge (corresponding to figure 1(c)) and (*b*) completed channels (corresponding to figure 1(d)). The microchannels in the pictures have channel width = 10 μ m, wall width = 10 μ m and channel height = 8 μ m.

Figure 3. Simulated distribution of an electric field when electroplating resumes after removal of the PR mold: (*a*) directions of the electric field; (*b*) distribution of electric potentials.

Figure 4. SEM pictures of microchannels: (*a*) parallel microchannels of different channel sizes (channel width = 10 and 20 μ m, wall width = 10 and 20 μ m, channel height = 8 μ m); (*b*) ends of the channels (channel width = 20 μ m, wall width = 20 μ m, channel height = 8 μ m).

the formation of hydrogen pits. The current density of 20 mA cm^{-2} was used, and the bath was maintained at room temperature.

At the initial stage, nickel was plated on the seed nickel surface not covered by PR and grew in the empty space of the PR mold, forming the side walls of the metal channels. As electroplating continued and reached the top of the mold, the metal began to form overhangs (figure 1(*b*)). When the neighboring overhangs grew close enough (e.g., $2-3 \mu$ m), electroplating was stopped. Through the small openings between the metal overhangs, the PR was easily removed with acetone (figure 1(*c*)). A cross-section of a sample at this stage is shown in the scanning electron micrograph (SEM) of figure 2(*a*), where the gap between the overhangs appears

smaller because the nickel was smeared during the sample polishing. After the plating resumed, the gap between the overhangs soon closed to form a sealed channel filled with an electrolyte (figure 1(d)). Inside of the hollow channel is equi-potential during electroplating, as illustrated by the electric field simulations in figure 3, and thus no further plating occurs inside the channel. This self-limited electroplating was an important motivation behind the presented fabrication method, because the channel inner geometry would remain as defined solely by the PR while the top layer would grow thicker and structurally stronger. The electrolyte trapped inside the channel when it was closed can be easily flushed with deionized (DI) water from ends of the channels before the channel was dried (figure 1(d)). Figure 4(a) shows an SEM

Figure 5. High-aspect-ratio microchannels (channel height = 43 μ m): (*a*) channel width (nominal) = 5 μ m, i.e., aspect ratio ~9; (*b*) channel width (nominal) = 10 μ m, i.e., aspect ratio ~4.

picture of parallel microchannels with different dimensions. A closeup picture at the entrance of the channel is shown in figure 4(b).

There are several benefits of the proposed method to fabricate microchannels. First, the microchannels are built monolithic, i.e., no bonding is used, simplifying the processes and avoiding the usual difficulties and drawbacks associated with bonding (e.g., surface conditions, processing temperature, alignment, etc). Second, it uses only one mask and a standard UV light source, allowing the use of a low-cost exposure system if needed. Third, electroplating is a low-cost, low-temperature procedure that can be added as the last step to the wafer fabrication without demanding modifications to the underlying device (e.g., IC). Also, one can lay out any arbitrary planar configuration of channels, keeping the kerf area and the contact pad areas free of the channel structures so that the subsequent steps of wafer dicing and wire bonding, respectively, remain standard for IC packaging. The presented fabrication method solves the problem of removing the mold material from inside of very long microchannels (e.g., the length-to-width ratio as large as a thousand), otherwise open only at the two ends of the channel [5, 14].

While the process detailed above proved the concept of the proposed microchannel fabrication using a moderately thick (~10 μ m) PR, an increased range of channel crosssections can be obtained as new types of PRs become available. For the mold, large height-to-width aspect ratios, vertical sidewalls and material compatibility with plating chemicals are usually desired. As an example, SJR 5740 PR (Shipley Ltd)—a positive PR of high viscosity and high transparency allows a high-aspect-ratio photolithography process using a standard UV light. Using this PR, we developed a multiplecoating process to produce an $\sim 40 \ \mu m$ tall plating mold. First, the wafers underwent a dehydration bake and a 10 min hexamethyldisilazane (HMDS) vapor prime. Then, the SJR 5740 was spin-coated at 2000 rpm. Edge bead removal was performed to ensure a flat PR surface. A 5 min relaxation was added between the coat and a subsequent soft bake. The relaxation step reduces film stress and improves uniformity in development. Next, the wafers were soft-baked on a hotplate, starting at 60 °C and then ramping up to 105 °C at a rate of 3 °C min⁻¹ before maintaining 105 °C for 10 more minutes. Without ramping the temperature during the soft

bake, the PR would shrink dramatically on the wafer, resulting in a poor uniformity. The wafers were cooled down in the atmosphere for 1-2 h before coating the second PR under the same conditions. While a single coating resulted in a $\sim 10 \,\mu m$ thick PR layer, a double coating produced 40–43 μ m. Following the soft-bake, the PR was exposed with a standard UV light (365 nm) through a photomask in a contact aligner (Karl Suss, 6.5 mW cm $^{-2}$). The plating molds were formed after development in an alkaline developer (1 part AZ-400K: 3 parts DI water). Typical exposure and development times ranged from 100 to 120 s and 15 to 20 min, respectively. A PR is usually postbaked to improve its adhesion to the substrate as well as its chemical resistance in the plating bath. However, the high-aspect-ratio PR mold pattern was found distorted by the postbake due to the high temperature. Consequently, the postbake was eliminated once the PR was developed. Using the photolithography process described above, mask features as small as 5 μ m were realized in the ~40 μ m thick PR with steep sidewalls. Following the plating procedures described in figure 1, microchannels taller than 40 μ m have been built while maintaining the nominal channel width and wall width at 5 or 10 μ m (figure 5). The physical integrity of microchannels was verified by injecting air into the inlet of the microchannels submersed in water and examining the escaping bubbles at the outlets under a microscope, as detailed in [10].

3. Application to electronic chip cooling

Unlike most other methods, the reported microchannels can be fabricated monolithically on the front side of the IC chip where the heat-generating devices reside, lowering the thermal resistance between the coolant and the heat source considerably compared with the conventional microchannel heat sinks bonded onto the backside of the wafer. A more important aspect of the present method, however, is the simplicity and economy it allows for building the eventual packaged electronic system. Building microchannels on the wafer in the last processing step prior to dicing would cost less than fabricating microchannels separately and bonding them to the IC wafer or chip. Since the presented channels can be formed on top of the final passivation layer on the wafer at low temperature, no alteration to existing IC processing steps is

Figure 6. Radially oriented microchannels (channel width = $5-15 \mu$ m, wall width = 5μ m, channel height = 40μ m): (*a*) photomask pattern, (*b*) SEM picture showing the center of the microchannels and (*c*) SEM picture showing the end of the microchannels.

necessary. Most interestingly, if air can be used as the coolant, as opposed to the usual liquid cooling, the overall electronic system can be designed much simpler. While the heat removal rate is considerably lower with air than liquid, the cooling system can be constructed much simpler. Empowered by the very high heat transfer rate of the present microchannels due to their material, size and location, we explore the unique possibility of using air as the coolant in this paper.

The present microchannels can be made with any arbitrary top configurations (i.e., layout) and varying cross-sectional areas, compared with the conventional microchannel heat sinks made of only straight channels of a constant cross-section. With this freedom, first, it becomes just a matter of mask layout to keep the wire-bonding pad areas free of channels. Second, one can design a more effective cooling by allowing more flow to potential hot spots rather than unilateral cooling of the chip surface. Third, by allowing gradually expanding channels, the ill effect of volume expansion can be reduced when air is used as a coolant. As an example, a radially oriented microchannel array has been fabricated. The mask pattern of the array is shown in figure 6(a), and the center and the outer end of the array are shown in the SEM pictures of figures 6(b) and (c), respectively. Air enters through the opening at the center and leaves through the openings at the outer edges of the array. As air temperature increases, the total cross-sectional area of the channels also increases and compensates for the volume increase. The compensation helps reduce the pressure drop by preventing the coolant from choking near the outlet of the channel. This design also simplifies the implementation by having only one air inlet. No return path for coolant is necessary since heated air is released to the atmosphere. The radially oriented, diverging microchannels optimize the use of pressure drop and simplify the packaging as well as the final electronic system.

4. Fabrication of a platinum resistive temperature sensor chip

4.1. Motivation

It would be the most direct way to confirm the cooling if one monitors the temperature distribution in real time with the sensors monolithically built right above the heating elements on chip. Among the temperature sensing techniques, we chose

Figure 7. Layout of the platinum temperature sensor array chip.

resistive sensors for its low cost in fabrication and simplicity in measurement. The resolution can be as high as several tens of microns, depending on the spatial layout of sensing units. Although not as sensitive as semiconductor (e.g., doped polysilicon) counterparts, the metal resistive sensors are sensitive enough for our purpose. We chose to implement platinum resistive temperature sensors for its low process temperature.

4.2. Design and fabrication of the temperature sensor chip

A platinum resistive temperature sensor chip was designed to measure the surface temperature distribution. Figure 7 shows the layout. The main goals of this temperature sensor chip were to thermally simulate the operation of a real IC chip and to measure the surface temperature distribution before and after the coolant was pumped through the microchannel array. Figure 8 describes the fabrication process schematically. The process starts with the deposition of a silicon nitride layer (1700 Å) on a silicon wafer. Mask #1 is used to pattern the backside nitride, and the inlet for the coolant is bulkmicromachined through the wafer using KOH. While the channel array in figure 6(b) was designed to work with an air inlet on top to ease the packaging, the tube directly on the channel would create an additional thermal path that would distort the analyses. To avoid the coolant tube becoming an extra thermal path, the design shown in figure 8 introduces the cooling air from the wafer backside. A 30% KOH solution at

Figure 8. Process flow to fabricate the Pt resistive temperature sensor chip.

80 °C was used, which provided an etching rate of 100 μ m h⁻¹. Etching was stopped when an $\sim 30 \,\mu$ m thick silicon membrane was left. Chromium 50 Å and nickel 200 Å were sequentially deposited on the front side using an E-beam evaporator and served as a thin-film heater. A low-temperature thermal oxide (LTO) (5000 Å) was deposited as a dielectric layer on the metal layer. Mask #2 was used to pattern the platinum resistors by the lift-off process using AZ 5214 PR. Before developing the PR, the wafer was dipped in chlorobenzene for 5 min to harden the PR surface and form an overhang, which helped the lift-off process by eliminating the step coverage of platinum. Titanium 150 Å and platinum 1000 Å were deposited on the LTO layer using the E-beam evaporator, the titanium promoting the adhesion. The LTO layer was patterned by mask #3 by RIE (CF₄ and O₂, 5:1, 200 W) to make openings for heater electrodes. AZ 1350 and mask #4 were used for the sequential lift-off process of aluminum metal contact lines. The thickness of aluminum was designed to be 1 μ m, so the thickness of the lift-off PR should be no less than 5 μ m to ensure a good result. After lift-off of the aluminum layer deposited by the E-beam evaporator, another oxide layer (2 μ m) was deposited on the wafer using plasma-enhanced chemical vapor deposition (PECVD). Mask #3 was used again to open all the bonding pads and electrodes by RIE. The etching rate was 1000 Å min⁻¹ for the plasma-enhanced chemical vapor deposition (PECVD) oxide.

An array of microchannels was built directly on the sensor chip in steps 9 and 10. First, a lift-off process was used with mask #5 to pattern a seed layer (Cr 50 Å, Ni 1500 Å) on the top of PECVD oxide. Thick PR (SJR 5740) was then spin coated on the seed layer to build a high-aspect-ratio plating mold for the microchannels (mask #6). Nickel was electroplated using the method described earlier. The last step was a series of

Figure 9. Optical image of the microchannel array near its center as viewed from the backside through an opening made through the silicon substrate. The opening and the channel array are slightly misaligned.

etching to open a path for the coolant to enter the center of the channel array: XeF_2 dry etching to remove the silicon membrane and the nitride, $HNO_3 + HCl$ (1:10) wet etching to remove Cr and Ni, followed by BOE etching of oxide. BOE attacks aluminum as well, so a layer of thin PR was coated on the front surface to protect the Al lines. It was important not to over etch the top PECVD oxide layer because the over etching led to a poor adhesion between the channel array and sensor chip. Figure 9 shows an optical micrograph of the channel array at its center, taken from the backside through the coolant inlet hole made through the silicon substrate.

4.3. Calibration of resistive temperature sensors

Figure 10 shows the calibration results of a fabricated platinum resistive temperature sensor chip in an iso-temperature oven. The figure contains the results of 20 temperature sensors, but most of the data are shown overlapping. The sensor was characterized by the linear relationship between temperature and resistance. The variation of resistance was less than 10 Ω , mainly from the variation of resistor size during the lift-off process and the variation of contact resistance during measurements. The data can be expressed by curve fitting into the following equation:

$$R = R_0[1 + a(T - T_0) - b(T - T_0)^2]$$
(1)

where R_0 is the resistance at the reference temperature T_0 (120 ± 5 Ω), resulting in $a = 3.91 \times 10^{-3} \text{ K}^{-1}$ and $b = 5.80 \times 10^{-7} \text{ K}^{-2}$. According to the design layout ($L = 40 \ \mu \text{m}$,

Figure 11. Optical micrograph showing several platinum resistive temperature sensors.

 $A = 0.6 \ \mu m^2$), the resistance of the platinum resistor was estimated to be $R_{\text{Pt}} \sim 76 \ \Omega$. The resistance of aluminum was only 1 Ω , two orders of magnitude lower, contributing little to the overall resistance. Also this error could be eliminated if the sensor was calibrated before being used.

Multi-meter was used to measure the change in the resistance with an observed resolution of 0.1 Ω at a sensing rate around 1 Hz. The frequency response was adequate since only steady-state heat transfer was dealt with in our experiment. The sensitivity, *S*, is defined as

$$S = \frac{\Delta R}{\Delta T} = R\alpha \tag{2}$$

where α is the temperature coefficient of resistance (TCR). The experimental sensitivity was 0.32 Ω K⁻¹. The measured resistance of the platinum resistor was higher than the designed value of 76 Ω at room temperature, likely because of the contact resistance between gold wires and bonding pads. After fabricating the sensor, a small current (5 mA) was applied to each resistor for 2 min to improve the contact between the platinum layer and the aluminum layer at the overlapping area (as shown in figure 11). The resistance would be reduced slightly and become more stable after the breakin. The sensing resolution of this platinum resistive sensor, 78 μm \times 78 μm in area, was computed to be 0.3 °C. During the temperature measurement, a very small current must be applied from the multi-meter to the resistor, leading to a self-heating of the resistive sensor due to Joule heating. However, the maximum temperature rise due to this effect was calculated to be less than 0.1 °C, small enough to neglect.

Figure 10. Calibration of Pt resistive temperature sensors in an iso-temperature oven.

Figure 12. Experimental setup for the cooling test (cross-section, not to scale).

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Figure 13. Deployment of temperature sensors and how they are used to obtain a temperature distribution. (a) Distribution of Pt resistors, numbered 1 to 20, allowing electric connections in one layer. (b) The measured temperatures from all the sensors are collected on one quadrant of the chip surface, considering a quadrantal symmetry. The numbers indicate the Pt resistors numbered in (a).

5. Chip cooling experiment

5.1. Experiment setup

The goal of the experiment was to verify that cooling occurs and to measure the thermal performance of the channel array using the temperature sensor chip, as illustrated in figure 12. The chip was heated by the thin-film metal resistor on it, the input power being the direct measure of heating. The temperature sensor chip was fixed in a Plexiglas block with a 5 min epoxy, thermally isolating the chip from the environment. The thermal conductivity of pure silicon is 148 W mK⁻¹, while that of Plexiglas is less than 2 W mK⁻¹. Neglecting the heat loss through the Plexiglas substrate, the power input to the heating resistor was considered close to the heat removal by the coolant at a steady state. The plated nickel channel array often detached from the PECVD oxide surface when the coolant was at a high pressure during the test. While the issue may be addressed by modifying fabrication in the future, we focused on thermal characterization by pressing the microchannel array to the substrate with a Plexiglas bar mounted on a *z*-direction stage. The plated nickel microchannel structure was strong and ductile enough to withstand this provision. A clear tube was glued to the inlet hole from the backside of the Plexiglas substrate with epoxy and connected to a nitrogen gas tank. A flow meter and a pressure gauge were mounted on the tank to display the flow rate and the inlet pressure, respectively.

The cooling experiment was carried out at a constant pressure drop of 50 psi (345 kPa) and a flow rate of 2.2 SCFH (17 ml s⁻¹). The surface of metal microchannel array was approximately at a uniform temperature during heating, and the ambient temperature was 25 °C.

5.2. Measurement of the surface temperature distribution

In laying out the resistive sensors that would collectively map the temperatures over the entire surface area, we considered a square chip that has a quadrantal symmetry. Figure 13(a)illustrates how the sensors were deployed, taking advantage of the symmetry to allow the independent electric connections to all the sensors with a single metal layer. Figure 13(b) shows a

Figure 14. Measurement of the temperature distribution. (*a*) Picture of the heater chip. A heater and an array of temperature sensors are below the square area of radial channels schematically shown in figure 6(a). The electrodes outside the channels are to access the sensors. (*b*) Measured temperature distribution during cooling (unit: °C). The temperature was uniform at 90 °C before cooling.

set of measured temperature data on one quadrant of the chip surface, based on our symmetry consideration. Figure 14 is a graphical representation of such a result.

5.3. Estimation of the cooling rate

The cooling rate is generally obtained from the inlet and outlet temperature of the coolant and its flowing rate. However, it was difficult to measure the temperature of heated air leaving the microchannel accurately because of the small scale. Although the temperature on chip below the channel exit could be measured, the temperature drop between the sensor and the air was estimated to be not negligible and easily affected by design and operation parameters. Instead, we obtained the cooling rate by a subtractive method described below. First, the rate of heating, i.e., the input power to the chip for Joule heating, was obtained easily from the input current and the resistance of the heating element. The rate of cooling by the flowing coolant, on the other hand, requires some considerations. Since the rate of heat loss from the heated chip to the surrounding (excluding the flowing coolant) depends on the temperature of the heater and the microchannel regardless of the coolant flows, such a power loss can be obtained under a no flow condition. After the system reaches a steady-state temperature with no coolant flow, the power loss to the surroundings P_{loss} should equal the input power P_{in} . Once the value of P_{loss} is known at a temperature, the power that is transferred to the flowing coolant (i.e., the rate of cooling by the coolant), P_{coolant} , at the same temperature can be obtained as

$$P_{\rm coolant} = P_{\rm in} - P_{\rm loss}.$$
 (3)

Figure 15 shows the cooling flux (i.e., power density to the coolant) obtained using the above method and the corresponding average temperatures measured on the heater chip by the temperature sensors. The cooling power about 6 W cm⁻² was obtained when the surface temperature was 90 °C.

6. Analyses of thermal performance

6.1. Governing equations and procedures

In order to analyze the thermal performance of a microchannel array, the flow rate must first be calculated. The pressure drop

Figure 15. Power density to the coolant with the variation of temperature.

of the coolant in a straight channel can be written as [2]

$$\Delta P = (2L/D)(\rho v^2)c_f \tag{4}$$

where *L* is the length of the channel, *D* is the hydraulic diameter of the channel, ρ is the density of the coolant, *v* is the mean flow velocity of the coolant and c_f is the friction factor. For a fully developed laminar momentum boundary layer, $\phi = c_f Re$ is constant and determined by the channel geometry as

$$\phi \equiv c_f \, Re = c_f \rho v D / \mu \tag{5}$$

where Re is the Reynolds number and μ is the dynamic viscosity of the coolant. Equation (4) can be rewritten as

$$\Delta P = 2\phi \mu L v / D^2. \tag{6}$$

Therefore, the total mass flow rate of the coolant \dot{m} in a straight rectangular channel heat sink is

$$\dot{m} = \rho v W D \alpha / 4 = \rho W \Delta P D^3 \alpha / (8\phi \mu L) \tag{7}$$

where *W* is the width of the cooled area by a channel array and α is the channel surface area enhancement = (channel surface area)/(heated area). The heat flow from the chip to the coolant *q* is represented as

$$q = (T_w - T_c)/\theta \tag{8}$$

where T_w is the temperature on the chip surface, T_c is the temperature of the coolant and θ is the thermal resistance.

The thermal resistance consists of a caloric thermal resistance due to coolant heating θ_{cal} , convective thermal resistance θ_{conv} and the thermal resistance between the base of the microchannel and the chip surface θ_{cont} . The thermal resistance θ_{cont} for the present microchannel is small, because the channel is directly on the heated front surface. For a constant-pressure constraint, the maximum temperature T_w (at the channel outlet) and minimum temperature T_c (at the channel inlet), the caloric thermal resistance θ_{cal} and the convective thermal resistance θ_{conv} are described as follows [2]:

$$\theta_{\rm cal} = (8\phi\mu L/\rho C_p \Delta P W) (D^{-3}\alpha^{-1}\eta^{-1}) \tag{9}$$

$$\theta_{\rm conv} = (1/k_c N u L W) (D\alpha^{-1} \eta^{-1}) \tag{10}$$

where C_p is the heat capacity of the coolant, k_c is the thermal conductivity of the coolant, η is the combination of temperature effectiveness of finned and prime surfaces and *Nu* is the Nusselt number.

The thermal performance of a straight channel based on Tuckerman's method can be analyzed with equations (7), (9) and (10) [2]. The temperature and pressure remain approximately constant when a liquid coolant is used for the usual microchannel cooling. However, when air coolant is used as in the present case, the temperature and pressure change significantly. Furthermore, the cross-sectional area of the present radially oriented channel varies along the channel length. Due to the change in the coolant properties and the diverging angle of the channel, the thermal performance of our radially oriented microchannel is analyzed numerically by dividing the channel into many short straight channels. Within each section, the temperature and pressure of the coolant and the cross-sectional area of the microchannel are assumed to be constant. The outlet temperature and pressure of each section are used as the inlet temperature and pressure of the next section. Iteration is carried out until the mass flow rate of every section is equal.

6.2. Parameters

As an example, a channel array with the pattern similar to figure 6(a) was analyzed, assuming nickel microchannels and nitrogen coolant and using the following parameters. As the channel diverges along the length, the channel width increased from 17 μ m to 39 μ m along its length, while the wall width and channel height were kept constant at 5 μ m and 40 μ m, respectively. The microchannel array was laid out radially with an overall diameter of 4000 μ m and the inlet hole diameter of 900 μ m. The array consisted of three branches of channels, designed for optimum performance. The inlet air temperature and the maximum chip temperature (at the outlet of the channel) were set at 20 °C and 90 °C, respectively. The pressure drop through the channel was set to be 30 psi (207 kPa). The values of Nu and ϕ were borrowed from those of a straight rectangular channel, justifiable because the difference in heat transfer between a straight rectangular

Figure 16. Distribution of temperature and pressure of the air coolant along the radially oriented microchannels (numerical simulation).

Figure 17. Distribution of velocity and density of the air coolant inside the radially oriented channel (numerical simulation).

channel and a diverging channel of 5° was known to be less than 7–8% [30]. Since the diverging angles of the present channels are less than 2.8°, the uncertainty from Nu and ϕ was considered smaller.

Figure 16 shows the temperature increase and the pressure decrease of the coolant as it flows along the channel. The temperature and pressure of the coolant vary somewhat linearly within a channel branch, but their slopes change abruptly where a new branch starts, reflecting the change of the divergent angle in the new branch. Figure 17 shows the density and velocity of the air coolant along the channel. The density of the coolant decreases because the temperature increases and the pressure decreases along the channel. However, while the mass flow rate is constant, the velocity does not vary monotonically. The coolant velocity decreases near the inlet as the cross-sectional area increases. But velocity increases near the exit. At branch 3, the divergent angle is small (about 1.2°), and the channels are almost parallel. Because coolant temperature increases sharply at this section as shown in figure 16, the gas expands faster than the channel diverges. In the middle section, the decrease in density balances with the increase in the cross-sectional area, resulting in a near-constant flow velocity.

The analysis showed that the rate of heat transfer, i.e. the cooling rate, was limited by the maximum velocity of the coolant at a given supply pressure. For this particular microchannel array, the maximum velocity was at the inlet, resulting in a heat removal capacity calculated to be 37 W cm^{-2} . Considering that a gas, not liquid, is used, this heat removal capacity is quite significant.

7. Discussion

By experimentally studying friction factors and the heat transfer of nitrogen gas flowing in microtubes of inner diameters ranging from 3 μ m to 81 μ m, Choi et al [31] observed that the friction factors were smaller than those predicted by the conventional correlation used for macro tubes in both laminar and turbulent flow regimes. Measured heat transfer coefficients were larger than those predicted by the conventional correlation. Flowing water in rectangular channels of 200–800 μ m × 700 μ m in cross-section and 45 mm in length, Peng and Peterson [32] observed that the transition from laminar to turbulent flow starts at $Re \sim 300$, developing to fully turbulent at $Re \sim 1000$. The Reynolds number of the present microchannel array varies from 300 to 1300, which is within the transition/turbulent flow regime of Peng and Peterson and perhaps the turbulent flow regime for our geometry. There has been no experimental study directly corresponding to the channel size and flow rate of this paper. In previous reports, heat transfer in microchannels is larger than what is predicted by the correlation obtained from macrochannels. However, the predicted heat removal capacity of 37 W cm⁻² is considered a conservative estimate.

When the channel length is increased, the analysis showed that the heat removal capacity was decreased because of the increase of a coolant specific volume near the end of the channel. For the cooling of the heating chip tested, cooling with a few sets of small radially oriented microchannels would be more advantageous than cooling with a single large set of radially oriented longer microchannels. For example, for the cooling of an 8 mm \times 12 mm IC chip, six sets of radially oriented microchannels with the size of 4 mm \times 4 mm can produce a heat removal capacity of about 37 W cm⁻².

Although not explored in this report experimentally, the diverging microchannels are expected to be promising for the cooling by a two-phase flow as well. The specific volume of water vapor is about 1000 times larger than that of liquid water. For the boiling convection in microchannels, the increase of a specific volume from the inlet as a liquid state to the outlet as a liquid–vapor mixture state would be great. For the parallel channels, the increase of a specific volume of coolant directly influences the coolant velocity and may cause choking near the end of the channel. However, for the radially oriented channels, the possibility of the choking problem would be decreased because of the increase of the cross-sectional area along the downstream of the channel.

8. Conclusion

A single-mask process was employed to fabricate metal microchannels 5–10 μ m in width and 10–40 μ m in height monolithically on the chip front side where heating occurs. By taking advantage of the smaller size and the freedom for any layout patterns that these microchannels allow, compared

with the well-known silicon bulk-etched microchannels for the liquid cooling (e.g., [2]), air cooling of a microelectronics chip has been explored. The air cooling has been confirmed by fabricating the microchannels on a heater chip and reading a temperature drop from 90 °C to 25–27 °C through an array of temperature sensors integrated on the chip. While the tested microchannel array provided a cooling of ~6 W cm⁻² in the experiment, a thermal performance analysis predicted a heat removal capacity of more than 35 W cm⁻² if the microchannels were further optimized. The compatibility with IC fabrication and the use of air as the coolant make the reported approach attractive for the system implementation of microelectronic chip cooling.

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