Low-Temperature Monolithic Encapsulation Using Porous-Alumina Shell Anodized on Chip

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Abstract—A thin-film encapsulation process, featuring low-temperature steps, hermetic sealing (preliminary), and RF-compatible shell, is reported. Uniquely attractive as compared with the existing MEMS packaging approaches is its capability to monolithically package metal microstructures inside a microcavity on chip in one continuous surface-micromachining process. The key for this process is a technique to fabricate a large freestanding porous membrane on chip by postdeposition anodization of thin-film aluminum at room temperature. The porous-alumina membrane allows for the diffusion of gas or liquid etchants through the nanopores to etch away the sacrificial material underneath, freeing the movable microstructures encapsulated inside the cavity. To seal the package, a thin film is deposited over the alumina shell whose nanoscale pores of a high aspect ratio (>30) do not allow any detectable penetration of the sealing material. The low-temperature (<300°C) encapsulation process produced a low-pressure seal (8 torr), monitored by a Pirani pressure gauge that also represents an encapsulated freestanding metal microstructure in the cavity. The thin-film package demonstrated a considerably low RF insertion loss of less than 0.1 dB up to 40 GHz.

Index Terms—Integrated packaging, low temperature, monolithic encapsulation, porous alumina, RF MEMS packaging, thin-film encapsulation.

I. INTRODUCTION

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OMPARSED to conventional approaches of packaging an individual MEMS device in metal or ceramic packages, wafer-level packaging—packaging the delicate MEMS devices on wafer before dicing—has long been accepted as the most effective way to reduce the back-end-of-line cost for a MEMS product. Hybrid wafer bonding [1]–[7], which employs direct surface bonding or an intermediate material to bond a separate capping wafer to the device wafer, is widely available in the industry as a mature wafer-level packaging approach. To address the main drawbacks in hybrid wafer bonding, such as excessive seal ring width, a thick profile, and the burden of aligning two wafers, various monolithic thin-film encapsulation processes [8]–[20] have been demonstrated, among which epitaxial silicon encapsulation is being used in commercial MEMS resonator products (www.sitime.com). Using thin-film processes, a sacrificial layer is deposited over an unreleased device, followed by the deposition of a thin film on top to form an encapsulation shell layer. Through etch holes opened in the encapsulation shell by lithography, the sacrificial materials are selectively removed by wet or dry etching, creating a cavity and freeing microstructures in it. The cavity is finally sealed by deposition of a micrometer- to several-micrometer-thick thin film on the encapsulation shell.

Permeable polysilicon, in situ deposited by low-pressure chemical-vapor deposition (LPCVD) under a certain condition [10], [13], and porous polysilicon, formed by postdeposition electrochemical etching [18], [20], were demonstrated as encapsulation shell materials with numerous submicrometer etch holes. The use of porous encapsulation shell allowed for fast removal of the sacrificial layers over the entire cavity area and lessened the issue of the internal deposition of the sealing material during the sealing process. Inspired by the success of a porous polysilicon shell in [13], we develop a new nanoporous thin film in this paper to meet with two essential requirements of packaging RF MEMS devices—low temperature and low RF loss. Low-temperature thin-film encapsulation has been demonstrated by using evaporated Al as a sealing film [21] or electroplated Ni as a package shell [16]. However, they are not suitable for RF packaging, as a conductive metal package introduces an RF loss path through the package. Dielectric materials deposited by sputtering [17] or plasma-enhanced chemical-vapor deposition (PECVD) [22] and spin-on glass [17] were used to package RF switches, and such packages showed RF losses much less than those of the conventional wafer bonding using solder [23], polymer bonding [24], or thermocompression [25]–[27].

Noting that aluminum can be deposited at a low temperature and that it can be anodized to a dielectric material of alumina with directional nanopores in a similar way as polysilicon [20], we have developed a process to form a freestanding porous-alumina membrane through postdeposition anodization for thin-film encapsulation [28] and reported some initial results in [29]. A similar method for fabricating a freestanding porous-alumina membrane for MEMS packaging was reported in a recent paper [30], where a different etching technique was used to form a porous-alumina membrane. Here, we consolidate the incremental results reported in [28] and [29]. Possessing the benefits of nanoporous thin-film encapsulation [20] and featuring a low-temperature process and extremely low RF loss, the
porous-alumina thin-film encapsulation process developed in this paper is potential to be a cost-effective packaging solution for various MEMS devices, particularly RF devices.

II. DESIGN AND FABRICATION

A. Fabrication of Porous-Alumina Membrane

Porous alumina is usually obtained by anodizing bulk aluminum foils in a variety of acidic electrolytes such as phosphoric acid, sulfuric acid, and oxalic acid. The typical pore structure, shown schematically in Fig. 1, is a hexagonal array of cylindrical pores (pore diameter: 10–300 nm) with a bottom $\text{Al}_2\text{O}_3$ barrier layer. In a typical (including commercial) porous-alumina process, the barrier layer is removed by polishing. For our application, however, the bottom $\text{Al}_2\text{O}_3$ barrier layer needs to be removed during the monolithic fabrication process to allow the etchants to diffuse through the nanopores and etch away the sacrificial material underneath. Because the wall thickness between the alumina pores is roughly twice the thickness of the barrier layer, removing the barrier layer by isotropic etching would also remove most of the alumina pore wall. Progressively reducing the anodization voltage [31], [32], or reversing the bias voltage immediately after the completion of the anodization etching of Al [33], requires accurate timing control to stop the etching and is not a reliable process for fabricating a porous-alumina membrane out of aluminum thin film deposited on a partially processed wafer surface.

It is possible to remove the barrier layer but not the alumina pore wall if the aluminum thin film is deposited on another conductive layer. When anodizing the Al thin film deposited on a silicon substrate [34] or an ITO-coated glass substrate [35], the conductive seed layer (silicon or ITO) allowed the anodization to continue, even after the etching front reached the interface, turning the entire Al thin film into porous alumina and transforming the otherwise thick and attached barrier layer into numerous thin arches. These thin arches can be removed by an isotropic wet etchant while only widening the pores marginally. Using a similar technique, we added a seed layer before the aluminum deposition and successfully perforated the bottom barrier layer in situ.

A process flow for fabricating the porous-alumina membrane is shown in Fig. 2. A stack of thin films on a silicon substrate, from the bottom to the top, consisted of a 0.3-μm PECVD oxide layer for insulation, a 1.5-μm amorphous-silicon (a-Si) sacrificial layer, a 1000/100-Å evaporated Ti/Au layer, and a 1-μm evaporated Al layer [Fig. 2(a)]. After being diced into 2-cm × 2-cm pieces, the samples were placed in a simple custom-made setup (Fig. 3) and anodized at a 40-V constant bias in a 0.3-mol/L oxalic acid at room temperature [Fig. 2(b)]. Although the anodization was done at the chip level in this paper, the same process can be scaled up to the wafer level once the challenge of keeping the anodization etching uniform across the wafer is overcome. Fig. 4 shows a typical current variation over time during the anodization etching. During the anodization etching, the current stabilized for a long period, indicating a process of stable pore growth. The pore morphology at the end of this stage can be observed from an SEM cross section shown at the top in Fig. 5(b). As the etching continues, the current started to increase rapidly, and it was accompanied with gas bubble generation, signifying that the etching front has reached the Au layer where electrolysis would occur. At the same time, the color of the surface started to change from opaque (i.e., the color of aluminum) to translucent and, finally, to transparent.
Fig. 4. Typical curve of current versus time in anodization etching. The anodization etching was performed on an approximately 2 cm × 2 cm sample at room temperature. The constant voltage used was 40 V.

Fig. 5. Porous-alumina pore morphology change at the end of anodization etching and after a wet isotropic etching to remove the bottom barrier layer. Only the box area of dashed lines in Fig. 2(b) is shown. (a) Schematic view. (b) SEM cross sections.

The etching was stopped when the surface layer became totally transparent. The current compliance was set below 100 mA to reduce the amount of gas bubbles generated at the interface of porous-alumina and Au layers, where the electrolysis between the 100-Å Au layer and the H$_2$O in the anodization etching solution took place at the end of anodization etching. Without limiting the current, the pressure built up by the excessive gas bubbles would have peeled the porous-alumina membrane off the Au layer. The structure of the bottom barrier layer after completion of anodization etching is shown in the middle SEM photograph in Fig. 5(b). A very thin (around 10-nm) arched barrier layer with a small void underneath was observed at the bottom of each pore. The 100-Å Au layer, sandwiched between the Ti adhesion layer and the Al layer, is resistant to the electrolyte during the anodization etching and essential to form an Al$_2$O$_3$ barrier layer consisting of numerous thin arches. Without the existence of the Au layer, the Ti adhesion layer would have been turned into an oxide layer by the electrolyte, which has a similar pore morphology as that of porous alumina. Thick Ti helps to distribute the etching current uniformly and thus achieve uniform pore growth across the entire area of the sample.

The arched thin barrier layer was then removed by a 5-wt% H$_3$PO$_4$ wet etching for 25 min, which also widened the pore to a diameter of 50 nm [bottom SEM photograph of Fig. 5(b)]. Next, the Au and Ti layers beneath the porous alumina were removed in Au etchant and Ti etchant (a mixture of NH$_4$OH, H$_2$O$_2$, and H$_2$O) in the area defined by a photoresist mask [Fig. 2(c)]. The photoresist mask was intended to remove the seed layers only in the cavity area so that the porous-alumina layer in other area was still attached to the substrate. Both the Au etchant and the Ti etchant have a very high selectivity to alumina, ensuring no further widening of the pores. It was found that if the Ti etchant was not well diluted (for example, NH$_4$OH:H$_2$O$_2$:H$_2$O = 1:1:2), a substantial amount of bubbles would be produced under the porous alumina, pushing and thus rupturing the porous-alumina membrane. Using a low-concentrated solution (NH$_4$OH:H$_2$O$_2$:H$_2$O = 1:1:8) reduced the amount of bubbles significantly, and the Ti layer was successfully etched away while the porous-alumina membrane was intact.

After the photoresist mask was stripped, the a-Si sacrificial layer was etched away by the XeF$_2$ gas, which diffused through the perforated pores [Fig. 2(d)]. An SEM cross section of the porous-alumina membrane thus obtained is shown in Fig. 6, where a 1.5-μm-thick air gap is visible below the alumina. A magnified view of the cross section of the membrane is shown in the inset. The transparent porous-alumina membrane exhibited a very good quality in terms of mechanical and structural purposes. Porous-alumina membranes as large as 2 mm a side were obtained without any cracks or wrinkles. Although not tested here directly, it is expected that the porous-alumina membrane can be fabricated on a wide variety of substrates, including glass substrates.

B. Encapsulation of a Surface-Micromachined Metal Microdevice

The hermeticity of the porous-alumina thin-film package was studied by monitoring the pressure change inside the package.
Fig. 7. Process flow for porous-alumina encapsulation of a Pt Pirani gauge.

The sealing of the package was achieved by depositing a PECVD low-stress nitride of 2.5 μm at 300 °C. The deposition pressure was 500 mtorr. The thickness of the sealing Si₃N₄ film was chosen to prevent physical contact between the package shell and the Pirani gauge when the package shell is deflected by the pressure difference as high as ~1 atm after sealing. The pressure–deflection relationship [36], [37] is given as

\[ p = \frac{3.41\sigma th}{a^2} + \frac{2.45Eh^3}{a^4} \]  \hspace{1cm} (1)

where \( p \) is the pressure difference applied on the shell; \( t \), \( 2a \), and \( h \) are the thickness, width, and deflection of the shell, respectively; \( E \) is the effective Young’s modulus of the package shell, which is dominated by that of sealing Si₃N₄ (~190 GPa). Neglecting the residual stress (i.e., \( \sigma = 0 \)) and assuming that the pressure inside the sealed cavity is 0.5 torr (= PECVD deposition pressure), we estimate that a 2.5-μm-thick Si₃N₄ shell that is 200 μm on a side would deflect around 1.9 μm. This deflection is smaller than the thickness (4 μm) of the photoresist sacrificial layer with a safety margin of two, ensuring that the spacing between the shell and the Pirani gauge is enough under reasonable operation conditions.

Then, the contact pads were opened to obtain electric connection to the Pirani gauge [Fig. 7(h)]. Note that the highest temperature in the current process was the deposition temperature of the sacrificial and sealing layers by PECVD. If they were deposited at a lower temperature, the thermal budget for the entire process would be determined merely by the lithographic steps.

C. RF Performance of a Porous-Alumina Thin-Film Package

Unlike the lithographically defined etch holes [8], [9], [11], [12], [14], [15], [17], [19], the nanopores with a very high aspect ratio in this paper do not allow the sealing material through an encapsulated metal Pirani gauge. The Pirani gauge is a freestanding surface-micromachined device and serves to represent a typical surface-micromachined metal structure and to read the vacuum level in situ. The use of Pirani gauge to monitor the pressure in situ was introduced in [7]–[9] and [16], and a polysilicon Pirani gauge has successfully been utilized for polysilicon encapsulation in [20].
to pass through them, effectively preventing its deposition inside the cavity. It was studied experimentally in [14] that the amount of sealing material (PECVD thin film) deposited inside the cavity was dependent on the aspect ratio of the release holes. The authors concluded that no internal deposition of the sealing material would occur if the aspect ratio (i.e., depth to diameter) of the release holes remains above four when the release holes are 0.35 \( \mu \)m in diameter. Given that an aspect ratio over ten (e.g., 0.5-\( \mu \)m-thick porous alumina with pores of diameter below 50 nm) can be easily obtained for the pores of porous alumina, it is anticipated that no sealing material would diffuse through the pores and deposit on the device surface inside the package. An experiment was carried out to confirm our claim. The test sample has a configuration, as shown in Fig. 8(a). The porous-alumina cavity was formed on a silicon substrate by removing the 5000-Å Ti sacrificial layer through the nanopores. Porous-alumina membranes of two different thicknesses, namely, 5000 Å and 1.5 \( \mu \)m, were fabricated. A pore aspect ratio ranging from 10 to 25 was obtained by changing the pore size through controlling the time in the widening process of the pores in 5-wt% \( \text{H}_3\text{PO}_4 \). After being sealed by a 5000-Å PECVD oxide deposition, as shown Fig. 8(b), the cavity was ruptured using a probe tip, and the thickness of oxide on top of the silicon substrate inside the cavity was measured by Nanospec with a thin oxide program (low limit: 20 Å). For all the samples tested, a “less than 20-Å” result was obtained, indicating that the porous-alumina shell effectively prevented the internal deposition of the sealing material during the sealing process.

To investigate the RF performance of the porous-alumina thin-film package, a coplanar waveguide (CPW) device was fabricated and packaged, following the fabrication process shown in Fig. 9. The process starts with 6000-Å thermal oxidation, as well as 3000-Å LPCVD silicon nitride deposition, to insulate the CPW line from the substrate [Fig. 9(a)]. A silicon wafer with high resistivity (> 2000 \( \Omega \cdot \text{cm} \)) was chosen to reduce the RF loss through the substrate. The subsequent liftoff process of Cr/Au 200/8000 Å formed a CPW line [Fig. 9(b)]. The dimension of CPW lines was designed and simulated using a commercial software (HFSS). The next step was PECVD depositions of 1-\( \mu \)m Si\( \text{O}_2 \) and 1.8-\( \mu \)m a-Si sacrificial layer [Fig. 9(c)]. Then, a 1000/100-Å Ti/Au seed layer was evaporated and patterned by the liftoff process [Fig. 9(d)], followed by 1-\( \mu \)m Al evaporation [Fig. 9(e)]. The wafer was diced into chips with a size of around 2 cm \( \times \) 2 cm. Following the procedure described earlier, the Al thin film on the entire chip was turned into porous alumina by the anodization etching [Fig. 9(f)], and the porous-alumina cavity was formed by removing the Ti/Au seed layer and the a-Si sacrificial layer sequentially [Fig. 9(g)]. A PECVD deposition of 1-\( \mu \)m low-stress silicon nitride sealed the device [Fig. 9(h)]. The final step was etching away all the films above Au in the electrical contact area.
III. RESULTS

A. Encapsulation of Surface-Micromachined Metal Microdevice

Shown in Fig. 10(a) is an optical microscope top view of the package with a Pt Pirani gauge encapsulated inside. The encapsulated Pirani gauge is clearly seen through the transparent porous-alumina shell and silicon nitride seal. From the angled SEM photograph of Fig. 10(b), the Pirani gauge is shown freestanding after the shell was intentionally ruptured. From the SEM photograph of Fig. 10(c), the cross-sectional details of all the layers, including the porous-alumina shell, the sealing nitride, and the Pirani gauge, could be observed on a cleaved sample. The cross-sectional view confirms that the Pirani gauge is suspended approximately 1 μm over the substrate.

The pressure inside the sealed cavity was measured from the encapsulated Pt Pirani gauge. We followed a procedure similar to that used for the polysilicon Pirani gauge [20] to calibrate the Pt Pirani gauge and monitor the internal pressure inside the package. The resistance-versus-current characteristics of a Pirani gauge were first obtained while it was encapsulated.

After breaking the seal, the entire sample was then placed in a pressure-controlling chamber, where the gauge was calibrated against known pressures. The pressure inside the sealed cavity, extracted by matching the resistance–current curve of the Pirani gauge while sealed with the calibration data (Fig. 11), was around 8 torr, a value that is much larger than the deposition pressure of the PECVD silicon nitride sealing film—0.5 torr. This discrepancy is speculated to be due to the outgassing from the residual photoresist left inside the package. A few ideas, including an extensive baking before the deposition of the sealing film, may be tried, if necessary in the future, to obtain a lower pressure inside the cavity. A preliminary evaluation of the package hermeticity was obtained from the thermal impedance changes of two sealed Pirani gauges, a method that was used in [7] and [16]. As shown in Fig. 12, the pressure inside the sealed packages has shown a less than 0.4-torr increase for 15 days. The testing was terminated after a short term because of logistic, rather than technical, reasons. We noted that one
of the devices showed a pressure decrease inside the cavity after 12 days. This could be due to the fluctuation of ambient temperature as the performance of the Pirani gauge is sensitive to the temperature change. Another possible reason is that the outgass from the traces of photoresist became absorbed on the interior surface of the porous alumina. A long-term hermeticity study of varying device configurations is desired in the future.

B. RF Performance of a Porous-Alumina Thin-Film Package

An optical microscopic top view of a fabricated device for evaluating the RF performance is shown in Fig. 13(a). A $160\times 300\mu m$ sealed cavity is seen in the middle of the photograph. The Au signal line encapsulated inside the sealed cavity is clearly visible through the transparent encapsulation shell, which is composed of $1.2\mu m$ porous alumina and $1\mu m$ silicon nitride thin films. The schematic views of the cross section of the devices along the $A-A'$ and $B-B'$ direction are shown in Fig. 13(b) and (c), respectively. The SEM cross section in Fig. 13(b) shows the porous alumina, along with the silicon nitride sealing film, suspending over the Au signal line by a gap of around $3\mu m$. Amorphous silicon was used to separate the encapsulation shell and the Au CPW lines in the feedthrough area. The cross section can be seen in the schematic figure of a $B-B'$ cross section and the SEM photograph in Fig. 13(c).

The influence of the package on the CPW lines was investigated by measuring the $S$-parameter matrix of a naked CPW transmission line and a packaged CPW transmission line. The measurement was conducted using an HP/Agilent 8510C network analyzer. Before the measurement, a calibration was performed on a calibration substrate using the probes and the software from GGB Industries, Inc. Fig. 14 shows the measured insertion loss ($S_{21}$), as well as the return loss ($S_{11}$), of both
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Fig. 15. Influence of feedthrough length on insertion loss. The package with 50-μm-long feedthrough was measured to have more insertion loss than the package with 20-μm-long feedthrough.

A porous-alumina thin film, obtained by the anodization etching of evaporated or sputtered aluminum thin film at room temperature, was discovered to be an excellent choice as an encapsulation shell for low-temperature on-wafer monolithic packaging. A surface-micromachining process, combined with anodization etching, was developed to fabricate a large free-standing porous-alumina thin-film shell. The barrier layer at the bottom of the nanopores was successfully perforated by extending the anodic etching with the help of a conductive seed layer and a short wet etching. A porous-alumina monolithic encapsulation was successfully developed to seal a surface-micromachined metal Pirani gauge at a low pressure (8 torr), and the package has demonstrated moderate hermeticity in a preliminary (i.e., short-term) characterization run. The influence of the porous-alumina thin-film package on the RF performance of MEMS devices was measured to be considerably low—less than 0.1-dB insertion loss up to 40 GHz.


