Fabrication of Very-High-Aspect-Ratio Micro Metal Posts and Gratings by Photoelectrochemical Etching and Electroplating

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Abstract—A high-yield fabrication process for dense arrays of very-high-aspect-ratio (VHAR) freestanding metal posts and gratings is developed. Silicon molds of regularly arranged through-holes or trenches are first fabricated by photoelectrochemical etching. By studying the etching parameters, including geometry constraint, current density and potential, electrolyte concentration, and etching time, we succeed to produce dense arrays of VHAR holes (depth \(= 610 \mu m\); diameter = 5 \(\mu m\); pitch = 14 \(\mu m\)) and trenches (depth = 320 \(\mu m\); width = 4 \(\mu m\); pitch = 8 \(\mu m\)) with yields higher than 99% on 2-cm² processing areas. The VHAR molds are then filled with metals using a new bottom-up electroplating technique, which features an intermittent vacuum degassing to remove the air and hydrogen bubbles from such deep and narrow voids during the plating. Zinc and nickel are successfully electroplated in high quality, and the freestanding metal structures are obtained by removing the silicon molds by XeF₂ etching. Obtained are maximum aspect ratios of 120 : 1 for posts (height = 600 \(\mu m\); diameter = 5 \(\mu m\); pitch = 14 \(\mu m\)) and over 60 : 1 for gratings (height = 250 \(\mu m\); width = 4 \(\mu m\); pitch = 8 \(\mu m\)) with yields higher than 99% on \(\sim 0.5 - 1\) cm² samples. [2011-0022]

Index Terms— Electroplating, high aspect ratio (HAR), photoelectrochemical (PEC) etching, vacuum degassing, very high aspect ratio (VHAR), 3-D microbatteries.

I. INTRODUCTION

THE FABRICATION of high-aspect-ratio (HAR) metal structures is of high interest for many applications of microelectromechanical systems. For an example, 3-D integrated circuits require an array of HAR metal (e.g., copper and nickel) vias formed through a silicon or glass wafer to interconnect multiple devices or circuit layers [1], [2]. Such HAR electrical feedthroughs offer significant improvements over 2-D packaging in response time, integration density, and reliability. For another example, dense arrays of HAR metal (e.g., zinc and nickel) posts were fabricated to serve as the electrodes of 3-D microbatteries [3], [4], which produce more energy and power than the traditional (i.e., 2-D) batteries on a given footprint area while sustaining high discharge rates [5]. For both the examples, one typically makes a mold by etching HAR through-holes and fills it with metals by electroplating. However, for the latter example (i.e., the 3-D battery), the mold should subsequently be removed so that the metals are released as freestanding 3-D electrodes.

To fabricate HAR metal structures as demanding as in the second example above, two key technological challenges must be addressed. One is how to form the mold with HAR through-holes that are only a few micrometers in diameter and in spacing. The other is how to fill such deep and narrow through-holes with no defect. Although deep reactive-ion etching (DRIE) has been widely used for through-wafer etching [1], [2], [6], the opening size is limited to several tens of micrometers, limiting the aspect ratio to mostly below 20 : 1. Through-wafer DRIE has other shortcomings, e.g., distortion in the hole diameter (i.e., nonvertical sidewall), local bowing due to the erosion of etching mask, and footing effect, which affect the quality of subsequent metal fillings. An alternative process for through-wafer etching is photoelectrochemical (PEC) etching, which can produce deep holes with an aspect ratio greater than 100 : 1 [7]. In this paper, we report an optimized PEC etching of silicon, which can produce dense arrays of very-high-aspect-ratio (VHAR) holes (depth = 610 \(\mu m\); diameter = 5 \(\mu m\); pitch = 14 \(\mu m\)) and trenches (depth = 320 \(\mu m\); width = 4 \(\mu m\); pitch = 8 \(\mu m\)) with yields higher than 99% on 2-cm² processing areas. On the other hand, such VHAR holes present an unprecedented challenge to fill them with minimal defects (e.g., voids) by electroplating. Although successful filling through a PEC-etched silicon mold has been reported [8], [9], one cannot assess the structural quality of the metal without removing the mold. Moreover, most such fillings were limited to \(\sim 200 \mu m\) in depth. To the best of our knowledge, there has been no report of a dense array of freestanding VHAR micro metal structures, which would demand a high-quality (i.e., defect free and stress free) filling.

So far, many electroplating techniques, most notably pulse plating [1], [2], [6], have been used to achieve a defect-free filling, but none reported an aspect ratio close to 100 : 1. In an effort to obtain dense arrays of VHAR metal structures, we have recently obtained promising preliminary results: dense arrays of VHAR (up to 85 : 1) freestanding nickel posts with
Fig. 1. Overall process to fabricate the VHAR micro metal posts and gratings, drawn schematically and not to scale. (a) Formation of sharp pits on silicon. (b) PEC etching of VHAR holes or trenches. (c) Deposition of a seed layer and filling the holes or trenches by vacuum-degassed electroplating. (d) Removing the silicon mold by XeF$_2$ etching.

III. FABRICATION

The overall fabrication processes used to fabricate the VHAR micro metal posts and gratings in this paper are schematically shown in Fig. 1. The four principal steps are formation of sharp pits [Fig. 1(a)], PEC etching of silicon [Fig. 1(b)], metal filling by electroplating [Fig. 1(c)], and silicon removal by XeF$_2$ etching [Fig. 1(d)].

The first step [Fig. 1(a)] is to form the sharp pits on a silicon surface needed to start the subsequent PEC etching. An n-type (100) silicon wafer with 40–60-Ω·cm resistivity was used, and ∼1500-Å SiO$_2$ was thermally grown on the surface. An array of squares or parallel lines of stripes were opened on the oxide layer using photolithography and a plasma etching, followed by a few seconds of dipping in buffered oxide etch (BOE), to serve as the etching windows for the subsequent KOH etching. Nominally (i.e., on the photomask), the square openings were 7 μm in size, and the stripe openings were 4 μm wide, 8 μm in pitch, and 25 mm long along the ⟨110⟩ direction. The silicon was then etched in 30% KOH at 78 °C for ∼15 min to form the V-shape pits, which served as the nucleation sites for the subsequent PEC etching.

After removing the SiO$_2$ layer in BOE, PEC etching started on a 2-cm-diameter circular area (i.e., ∼3 cm$^2$) of silicon [Fig. 1(b)], dictated by the etching apparatus. A platinum sheet served as the cathode, and the sample was illuminated from the
back side using a high-power light source (Marubeni America Corporation) operating at 870 nm. The silicon was exposed to the electrolyte in a 2-cm-diameter circle. The electrolyte was 5-wt% hydrofluoric acid (HF) in deionized (DI) water (26 mL of 49% HF in a total volume of 300 mL) for the square patterns and 2.5-wt% HF in DI water (13 mL of 49% HF in a total volume of 300 mL) for the stripe patterns. A few droplets of a wetting agent (Kodak Photo-Flo) were added to the electrolyte to help remove the hydrogen bubbles generated during the etching, which is very important for VHAR etching. For the PEC etching, a current density of 2 mA/cm$^2$ was used for the square patterns, and 6 mA/cm$^2$ was used for the stripe patterns, while the anodic voltage was independently kept constant at 2 V. After growing to a desirable depth into the silicon, the pores or trenches were opened from the back side by DRIE.

In preparation for the electroplating [Fig. 1(c)], all the surfaces were covered with a 2000-Å SiO$_2$ by thermal oxidation to prevent metal growth on them during the subsequent electroplating. Then, the sample was broken into ∼0.5- and ∼1-cm$^2$ rectangular pieces for posts and gratings, respectively, to satisfy the 3-D microbattery project that the process was developed for. Using the small samples, a 100-Å/1000-Å Ti/Ni was deposited on the back side in an e-beam evaporation system (CHA Mark 40) as a seed layer, and an ∼30-μm-thick nickel was grown by electroplating at 5 mA/cm$^2$ for 6 h to seal the openings and form the base plate for the eventual freestanding 3-D structures. Next, the back side of the mold was covered with a red polyplating tape 350F (Echo Engineering and Production Supplies, Inc.) to passivate the nickel surface on the back side. This nickel, exposed at the bottom of the deep pores or trenches, then serves as the seed layer for the subsequent bottom-up electroplating to fill the mold. For the nickel, a commercially available plating solution (Technic Inc.) was used, and a nickel sheet was used as the counter electrode during the electroplating. For the zinc, a plating solution was prepared by dissolving zinc sulfate (240 g), ammonium chloride (15 g), aluminum sulfate (30 g), and saccharin (1 g) in 1 L of DI water [13], and a zinc sheet was used as the counter electrode. To fill the VHAR silicon molds, we have developed an intermittently vacuum-degassed electroplating technique, described in the following.

An important challenge against the mold-based fabrication of metal microstructures has been the gas trapped in the mold, which would introduce voids in the metal or even block the growth of the metal. So far, most known electroplating processes use a small amount of surfactant to help wet the plating mold. This simple method works well for relatively low aspect ratio and even HAR molds in some cases but unfortunately not for VHAR molds (e.g., 100:1). Alternatively, vacuum degassing has been known to be effective in removing the gases during electroplating. An early solution [11] was to evacuate the air space above the plating bath and maintain the pressure lower than the atmospheric pressure during the electroplating. Although a smooth and pit-free surface was reported on a flat surface (i.e., no holes), the evaporation of water was significant due to the vacuum bath, requiring a complex apparatus and operation for feedback control. More importantly, if adopted for the electroplating of VHAR molds, this vacuum-plating method would hurt rather than help because the vacuum would make even a small amount of gas expand to form bubbles and block the electroplating in the mold. Another degassing method [12] repeated vacuum and venting several times before electroplating started, drawing the initially trapped air bubbles out from the cavities and dislodging them from the surface. However, without an effective degassing during the electroplating, it was difficult to remove the hydrogen accumulated after the plating process started. Unlike all the existing vacuum-electroplating methods, our technique, first introduced preliminarily in [10], uses an intermittent degassing mechanism, as schematically shown in Fig. 2. To remove the air initially trapped when the mold was immersed in the plating solution, the pressure in the plating bath is lowered before electroplating started. Once the electroplating starts, on the other hand, the bath is evacuated and vented periodically (e.g., hourly) to remove the hydrogen accumulated. Both nickel and zinc were electroplated using this technique.

Finally, to obtain the freestanding micro VHAR metal structures, the silicon molds were removed by a gas-phase XeF$_2$ etching at 3000 mtorr for ∼1.5 h (60 cycles of a 90-s pulse). The thin SiO$_2$ surrounding the metal sidewalls was also removed during the XeF$_2$ etching mostly due to the poor adhesion to the metal surface and not-optimized etching selectivity [Fig. 1(d)].

III. RESULTS AND DISCUSSION

A. PEC Etching of the Pore Structure

The PEC etching of pores has been widely studied, and aspect ratios over 100:1 have been reported multiple times [7], [14], [15]. However, most reported etching depths were limited to less than 500 μm. According to the discussion in [16], the maximum obtainable pore depth can be around 500 μm, using a low-concentration electrolyte, low temperature, and long etching time. The main limitation is a long diffusion of the electrolyte as the pores grow deeper. In this study, first, we performed the PEC etching using an ∼5-40-μm-thick silicon wafer at a current density of 2 mA/cm$^2$. Fig. 3(a) shows the cross-sectional picture of the 530-μm-deep pores formed after 750 min of etching while maintaining the pore diameters at ∼5 μm, which is similar to the maximum depth reported in [10]. We encountered no fundamental reason for the pores to not grow deeper as long as a proper current density is used. Therefore, we further performed the PEC etching using a 680-μm-thick silicon wafer to explore deeper pores, using the same current density of 2 mA/cm$^2$. Fig. 3(b) shows 610-μm-deep pores formed after 960 min of etching while maintaining the same pore diameters of ∼5 μm. Although it may seem that the pores can grow even deeper by simply increasing the etching time, further exploration revealed that the pores tend to degenerate eventually. Fig. 3(c) shows such a limitation—degenerated pores after growing ∼630 μm deep at 1140 min of etching. As the pores grow deeper, the electrolyte concentration at the etching front continues to decrease, causing the degeneration eventually, as reported in [16]. A possible solution is to use a current density adjusting as the holes deepen or to devise a mechanism to refresh the electrolyte, preventing the rapid decrease in electrolyte concentration.
B. PEC Etching of the Trench Structure

Unlike deep pores, deep trenches by PEC etching have not been studied much until recently [17]–[19]. In addition to the need of V-grooves (rather than reverse pyramids) for nucleation, the etching of trenches is different from that of pores in terms of the required current density. For pores, the current density $J$ can be much smaller than the critical current density $J_{ps}$, which is exclusively dependent on the electrolyte concentration. For example, the pores in the previous section were formed with $J = 2 \text{ mA/cm}^2$ and $J_{ps} \approx 43 \text{ mA/cm}^2$ (i.e., 5-wt% HF). However, one cannot form deep trenches properly under the same condition. Fig. 4 shows the result with $J = 2 \text{ mA/cm}^2$ and 2 V in 5-wt% HF. Not trenches but some randomly located pores were formed. After detailed examinations, we explain the
failure as follows. Because the etching current density was too small \((J = 2 \text{ mA/cm}^2)\) compared with the critical current density \((J_{ps} = 43 \text{ mA/cm}^2)\), the initial PEC etching could not form complete trenches along the nucleation grooves, resulting in many discrete pores starting to form in the grooves, as described schematically in Fig. 5(a) viewed from the top. To succeed, the pores must be dense enough to merge as a continuous trench, as shown in Fig. 5(b), which would require a higher current density. In our study, a ratio of \(J/J_{ps} = 0.4\) was found good enough to etch 4-\(\mu\)m-wide trenches spaced by 4 \(\mu\)m (i.e., a pitch of 8 \(\mu\)m). Following this ratio, we applied \(J = 6 \text{ mA/cm}^2\) at 2 V, using 2.5-wt% HF \((J_{ps} \approx 15 \text{ mA/cm}^2)\). Fig. 6(a) and (b) shows 220- and 320-\(\mu\)m-deep trenches after etching for 540 and 840 min, respectively. The obtained trenches were found to have good uniformity (in width, depth, and sidewall smoothness) over the entire processing area (\(\approx 3 \text{ cm}^2\)).

Compared with the deep pore etching, the deep trench etching degenerates more easily, which limits the etching depth. As described previously, the trench etching is more sensitive to the current density and the ratio of \(J/J_{ps}\). Although an optimized current density can alleviate the degeneration, \(J_{ps}\) changes appreciably as the pores grow deep. If \(J\) is kept constant, the trenches will modify their widths according to the changing \(J/J_{ps}\). Once the parameters deviate from a stable etching condition, some adjacent trenches will start to merge, and others branch out and stop growing eventually. Another issue limiting the etching depth is that the etching rate in 2.5-wt% HF is much lower than that in 5-wt% HF. Currently, for the 5-wt% HF electrolyte \((J_{ps} = 43 \text{ mA/cm}^2)\), our apparatus could not provide a stable and high enough current density to fulfill a ratio of \(J/J_{ps} = 0.4\) during the etching, mostly due to the insufficient light intensity. We expect deeper trenches in the future by utilizing an adjustable current density, devising an electrolyte refreshment mechanism, and resorting to a more powerful light source.

C. Freestanding Micro Metal Posts

To fill the VHAR molds (e.g., Figs. 3 and 6), the existing electroplating techniques were unsatisfactory, mostly because the gases trapped inside the narrow and deep voids become more difficult to remove as the aspect ratio increases. Successful fillings of HAR holes and release of HAR metal structures have been reported [20], [21], but the aspect ratios were mostly lower than 20:1. Although filling of VHAR holes
Fig. 6. Formation of deep trenches (width = 4 μm; pitch = 8 μm) by PEC etching of silicon under the conditions detailed in the main text. (a) After 540 min of etching (depth = 220 μm; aspect ratio = 55:1). (b) After 840 min of etching (depth = 320 μm; aspect ratio = 80:1).

Fig. 7. HAR metal posts obtained using regular electroplating (i.e., without vacuum degassing), showing many missing posts. (a) Zinc posts (height = 250 μm). (b) For an intended height of 500 μm, only a few short posts were found standing.

Fig. 8. Dense array of 500-μm-tall freestanding Zn posts (diameter = 5 μm; pitch = 14 μm; aspect ratio = 100:1) processed over a 0.5-cm² rectangular sample with 99% yield.

(200-μm-deep holes of 100:1 aspect ratio) has been reported [8], the metal was not released as freestanding structures. While the yield of through-hole etching is easily estimated by inspecting the openings on the opposite side, the quality of filling cannot be assessed reliably until the mold is removed. Fig. 7 shows the results for micro posts without using a vacuum degassing. Fig. 7(a) is for Zn posts made from a mold with 250-μm-deep pores. Although the aspect ratio shown here is not very high (< 50:1), many posts were found missing, bent, and having different heights. Fig. 7(b) is for Ni posts made from a VHAR mold of 500-μm-deep pores of 100:1 aspect ratio. Few posts were found standing, and they were even shorter than 100 μm.

Using the intermittently vacuum-degassed electroplating, we were able to obtain a high-quality filling of both zinc and nickel. To obtain high hardness and low internal stress, relatively low current densities of 5–30 mA/cm² for nickel and 15–30 mA/cm² for zinc were used. Fig. 8 shows the VHAR zinc
posts (diameter = 5 μm; pitch = 14 μm; height = 500 μm; aspect ratio = 100 : 1) freestanding after XeF₂ etching of the silicon mold. After placing the mold in the plating bath and before the electroplating, the plating tank (the gas above the solution, to be exact) was pumped out to remove the air trapped in the pores. The plating started at a lower current density of 15 mA/cm² for 2 h and continued at a higher current density of 30 mA/cm² for 10 h at a room temperature. During the electroplating, the plating tank was pumped out hourly to remove the H₂ accumulation. Fig. 9 shows the VHAR nickel posts (diameter = 5 μm; pitch = 14 μm; height = 600 μm; aspect ratio = 120 : 1) freestanding after XeF₂ etching of the silicon mold. In this case, the plating consisted of three sequential phases: 5 mA/cm² for the first 20 h, 10 mA/cm² for the middle 20 h, and 30 mA/cm² for the last 8 h. The degassing was performed every 2 h during the plating. The lowest current density in the beginning was for slow H₂ generation at the bottom of the pores, where the gas is most prone to be trapped. As the metal starts to grow up from the bottom and the pores become shorter, the current density was raised to increase the plating speed and reduce the total plating time (i.e., 48 h). Compared with our previous result of the micro metal posts [3], the aspect ratio has increased significantly (25 : 1 → 120 : 1), as has the yield (∼ 40% → ∼ 99% over a similar sample size around 0.5 cm²) and uniformity, which is critical for many applications.

Note that the metal posts (Figs. 8 and 9) appear irregular compared with the holes of the silicon mold (Fig. 3). We would like to emphasize that the deformation was caused by the “postprocessing” performed to prepare cross-sectional surfaces for the visualization rather than by the inherent properties of the plated metal. First, note that the posts are a metal and go into plastic deformation above a yield stress, while the silicon mold is a ceramic and returns to the original shape after any deformation (unless broken). Most of all, the process of making a cross-sectioned sample deformed some of the electroplated metal structures. During the procedures of cleaving the metal-filled mold samples and polishing their cleaved side surfaces, the metals must have experienced strains above their yield points. Note that the cleaving caused a strain of more than ∼5% needed to fracture silicon; this is much larger than the yield strain of most metals (e.g., 0.02% for nickel). While silicon (a ceramic) goes through a large strain for the cleavage and comes back to the original shape with no memory, metals build a residual stress in them when they deform plastically and return to the original shape. When the VHAR structures are freed by removing the silicon, the built-in stress in them would make them bend. In addition, the SEM process caused an image distortion because the VHAR posts bent under the high electric field inside the SEM chamber. For example, the posts in Fig. 8 looked much straighter under different viewing angles.

D. Freestanding Micro Metal Gratings

Next, we filled the trench mold [Fig. 6(b)] with nickel by electroplating and released it as freestanding gratings (or plates) by etching silicon. Fig. 10 shows the obtained nickel gratings (width = 4 μm; pitch = 8 μm; height = 250 μm; aspect ratio > 60 : 1) with a 100% yield and a very good uniformity over the entire sample area of ∼1 cm². During the plating, a current density of 10 mA/cm² was applied for 20 h, and vacuum degassing was applied hourly. For our 3-D battery applications, this type of electrodes is expected to provide a better mechanical stability over the post electrodes while maintaining a similar battery performance.

E. Further Discussion

The PEC etching setup used in this paper was developed in-house for laboratory research and can process samples up to 2 cm². The electroplating setup was also developed in-house and produced VHAR metal structures of ∼0.5 and 1 cm² in area—the sample size needed for our 3-D microbattery research [3], [4]. All the results in this paper, including the yields, have been based on 20 samples produced for the 3-D microbattery project through at least 15 times of different fabrication runs. To our knowledge, no wafer-scale apparatus is commercially available yet that can produce our reported results.

Material properties of the VHAR metal structures, e.g., hardness, stress, and electrical conductivity, are important for most applications. Full measurement and characterization have not been attempted in this paper because of the challenges associated with their small features (e.g., diameter = 5 μm and pitch = 14 μm). Instead, we inquired into the material properties through high-magnification visual inspections.
Dense arrays of micro metal posts and gratings of VHAR were fabricated with a high yield (> 99% on an ∼0.5–1-cm² sample) by a well-tuned PEC etching of silicon and a custom-developed electroplating of metals. Silicon molds with through-holes (diameter = 5 μm; pitch = 14 μm; depth = 600 μm; aspect ratio = 120 : 1) and trenches (width = 4 μm; pitch = 8 μm; depth = 320 μm; aspect ratio = 80 : 1) have first been prepared by PEC etching with a high yield (99% on 2-cm² processing areas). By developing an intermittently vacuum-degassed electroplating and filling the deep voids in the VHAR mold using the new plating technique, after removing the mold, we were able to obtain freestanding micro metal posts of aspect ratio up to 120 : 1 and gratings over 60 : 1. Compared with the previous report, the aspect ratio of the posts was significantly improved (25 : 1 → 120 : 1 for posts). Often more importantly for applications, e.g., 3-D microbatteries, the processing yield and structure uniformity were dramatically improved (∼40% → ∼99%). This reporting of the micro metal gratings is the first to our knowledge. Our immediate goal is to utilize the technology to fabricate VHAR zinc posts and gratings as 3-D electrodes to develop zinc–air microbatteries of higher energy density and discharge rate.

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REFERENCES


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