A LOW TEMPERATURE VACUUM PACKAGE UTILIZING POROUS ALUMINA THIN FILM ENCAPSULATION

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ABSTRACT

We report a monolithic thin-film encapsulation method that satisfies the most popular requirements for on-wafer packaging: low temperature, low cost, hermetic, and RF compatible. The key for this new nano-porous thin-film encapsulation method is the technique to produce a large free-standing porous alumina membrane on-chip by post-deposition anodization of aluminum at room temperature. A porous alumina membrane allows for the diffusion of gas or liquid etchants through the nano-pores into the cavity to etch the sacrificial material, freeing the movable structures encapsulated inside. Subsequent vacuum sealing was achieved by depositing a thin film over the nano-porous alumina shell in a vacuum deposition tool, with no detectable penetration of the sealing material owing to the nano-pores with a high aspect ratio (> 30). The process, done at a low temperature, produced a hermetic vacuum seal and demonstrated an exceptionally low RF insertion loss: < 0.1 dB up to 40 GHz.

1. INTRODUCTION

For MEMS on-wafer packaging (i.e., packaging all the MEMS devices on one wafer at the same time rather than on an individual die), although hybrid wafer bonding [1-3] has been being widely used in industry, monolithic thin-film encapsulation [4-8] has long been considered to be potentially more effective in simplifying the packaging procedure and thus reducing the cost of a MEMS product. Carried out on a single wafer by adding extra steps to the surface micromachining process used to construct the device, the monolithic thin-film packaging process has several main advantages over wafer bonding: (1) It employs surface micromachining batch fabrication processes, avoiding the need for aligning two wafers and the challenges of bonding on processed (i.e. not smooth) surfaces. (2) It eliminates the seal ring, increasing the number of available dice per wafer. (3) Having much lower topography, a thin-film package allows for post-encapsulation processes for additional MEMS or IC steps.

Various thin-film packaging processes have been demonstrated to encapsulate a wide variety of MEMS devices [4-11]. Prevalently, the sacrificial layers were removed by wet or gas etchants through a limited number of micrometer-sized etch holes *lithographically* opened in the encapsulation shell, which were subsequently sealed by a micrometer-thick thin film to form a sealed cavity. Permeable polysilicon, *in situ* deposited by LPCVD at a certain condition [8, 9], and porous polysilicon, formed by post-deposition electrochemical etching [4, 12], were developed as encapsulation shell materials with numerous sub-micron etch holes, enabling fast removal of the sacrificial layers while preventing the internal deposition of the sealing film. However, as most other monolithic encapsulation methods do, they still used high process temperature, limiting their use in such applications as RF MEMS, where metal (e.g., gold, aluminum) is frequently used to build the devices and cannot withstand any high temperature processes.

What is desired is a nanoporous encapsulation shell that can be fabricated at low temperature and ideally is composed of a dielectric material to pair well with RF. Such a material was found in porous alumina formed by anodization etching out of aluminum thin film deposited by evaporation or sputtering. Possessing the features of nanoporous thin-film encapsulation [4], the new thin-film encapsulation process in this paper offers a low-cost and robust packaging solution for various surface-micromachined devices, especially RF switches and resonators.

2. FABRICATION OF POROUS ALUMINA MEMBRANE

The typical pore structure of anodized porous alumina is a hexagonal array of cylindrical pores (pore diameter: 10-300 nm) with a bottom Al_2O_3 barrier layer. For the application of thin-film encapsulation, this barrier layer needs to be removed to allow the diffusion of etchants through the nanopores to etch away the sacrificial material.

A technique similar to [13] was used to *in situ* perforate the bottom barrier layer of porous alumina pores. The geometry of the sample tested for the fabrication of a porous alumina membrane is shown at Fig. 1(a). The thin film stack on a silicon substrate, from the bottom to the top, consisted of a 0.3 µm PECVD oxide layer for insulation, a 1.5 µm a-Si (amorphous silicon) sacrificial layer, an 1000/100 Å evaporated Ti/Au and a 1 µm evaporated Al layer. The anodization etching was performed at 40 V constant bias in a 0.3 M oxalic acid at room temperature as shown in Fig. 1(b). During anodization etching, the current stabilized for a long period, indicating a process of stable pore growth, and then suddenly started to increase steadily accompanied with gas bubbles generation, signifying that the etching front has reached the Au layer and, due to the existence of H_2O in the electrolyte, the electrolysis started to generate O_2 gas. At the same time, the color of the surface changed from opaque (i.e., the color of Al), to translucent and finally to transparent. The

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etching was stopped when the thin film became transparent. The structure of the bottom barrier layer after anodization etching was completed is shown in the middle SEM picture in Fig. 2(b). A very thin arched barrier layer (around 10 nm) with a small void underneath was observed at the bottom of each pore. The arched barrier layer was removed by a 5 wt% H_3PO_4 wet etching for 25 minutes, which also thinned down the pore wall to a diameter of 50 nm (bottom of Fig. 2(b)). The 100 Å Au layer was essential to form the numerous thin arches. Without the existence of Au layer, the Ti adhesion layer would have been turned into an oxide layer by the electrolyte, which has similar pore morphology as that of porous alumina. Next, the Au and Ti layers beneath the porous alumina were removed in Au etchant and Ti etchant (NH_4OH:H_2O_2:H_2O=1:8) in the area defined by a photoresist mask (Fig. 1(c)). After the photoresist mask was stripped, the a-Si sacrificial layer was etched away by the XeF_2 gas, which diffused through the perforated pores (Fig. 1(d)).

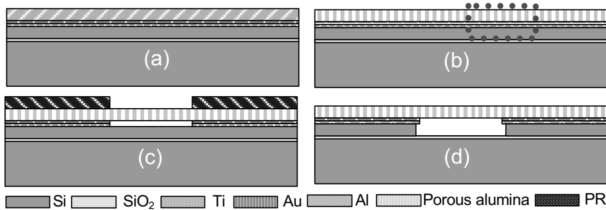

Figure 1: Fabrication process flow of a porous alumina membrane. Anodization etching was done at step (b).

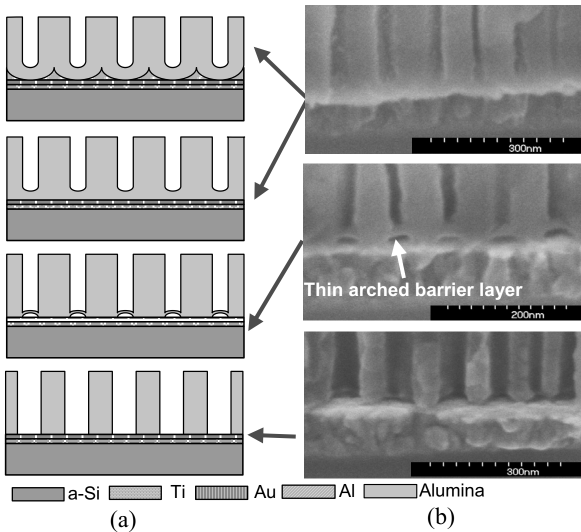

Figure 2: Pore morphology change at the end of anodization etching. Only dashed line area in Fig. 1(b) is shown. (a) Schematic view. (b) SEM cross sections.

A SEM cross section of the porous alumina membrane thus obtained is displayed in Fig. 3, where a 1.5 µm thick air gap is visible below the alumina. A magnified view of the cross section of the membrane is presented in the insert. The *transparent* porous alumina membrane exhibited a very good quality in terms of mechanical and structural purposes. Porous alumina membranes as large as 2 mm a side were obtained without any crack or wrinkle.

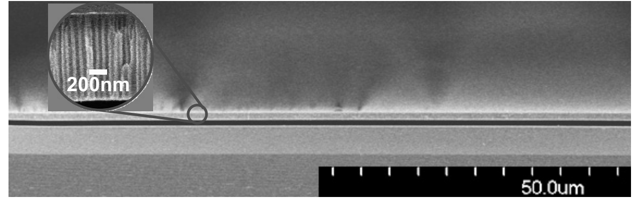

Figure 3: SEM cross section view of a porous alumina membrane.

3. ENCAPSULATION OF PIRANI GUAGE

The hermeticity of encapsulation with the porous alumina thin film was studied by monitoring the pressure change inside the package through an encapsulated metal Pirani gauge, a free-standing device representing the typical surface-micromachined metal structures as well as reading the vacuum level *in situ*.

The process flow is illustrated in Fig. 4. After the fabrication of a metal Pirnai gauge, a 4 µm photoresist sacrificial layer was deposited and patterned to define the gap between the Pirani gauge and the thin film. The photoresist was hard baked at 120 ^oC in an oven for 20 minutes to reduce the outgassing during the subsequent processes, followed by an O_2 plasma etching for 2 minutes to roughen the surface for the purpose of improving the adhesion of metal layers subsequently deposited. The thin-film cap above the photoresist sacrificial layer consisted of sputtered 3200 Å Ti and evaporated 100/15000 Å Au/Al layer (Fig. 4(a)). The anodization etching of Al was performed on a 2 cm by 2 cm chip (Fig. 4(b)). The current compliance was set below 100 mA to reduce the amount of gas bubbles generated at the end of anodization etching. Next, by using a photoresist mask, the alumina pores over the cavity area were widened by 25 minutes 5 wt% H_3PO_4 etching and the Ti/Au seed layers were removed through the pores. The photoresist mask, along with the photoresist sacrificial layer below the porous alumina, was removed by O_2 plasma etching (Fig. 4(c)). Afterwards, the a-Si sacrificial layer under the Pirani gauge was removed by XeF_2 plasma dry etching. The vacuum sealing of the package was performed by depositing a PECVD low stress nitride of 2.5 µm at 300 ^oC. The entire packaging process can be carried out at room temperature if a room-temperature sacrificial layer and sealing layer are used. Then, the contact pads for electric access to the Pirani gauge were opened (Fig. 4(d)).

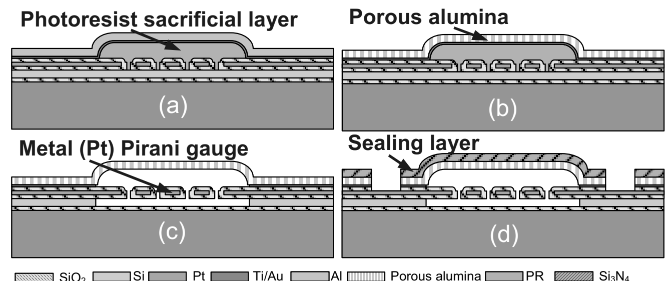

Figure 4: Process flow of vacuum encapsulation of a metal Pirani gauge.

A package was intentionally ruptured to expose the free-standing Pt Pirani gauge inside (Fig. 5(a)) as well as each layer of the encapsulation shell (Fig. 5(b)). The Pirani gauge can be seen free-standing in both pictures.

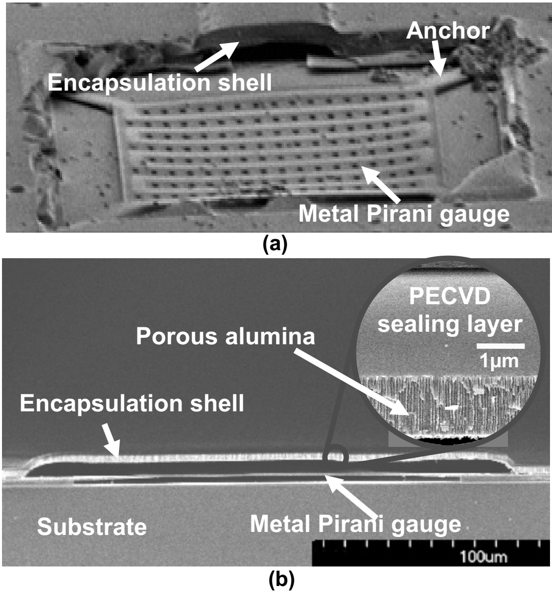

Figure 5: (a) A porous alumina package intentionally ruptured to expose the Pirani gauge. (b) Cross section showing the silicon nitride sealing layer, the porous alumina layer as well as a suspended metal (Pt) Pirani gauge.

The pressure inside the sealed package was obtained by matching the resistance-current curve of the sealed Pirani gauge with the resistance-current curves of the gauge calibrated at different pressures. Plotted in Fig. 6 is the data measured from a package. The pressure inside the sealed device was found to be around 8 Torr, a value much larger than the deposition pressure of 0.5 Torr. This discrepancy is likely due to the outgassing of the photoresist residue inside the package. The hermeticity of the packages was measured from the thermal impedance changes of two sealed Pirani gauges. As displayed in Fig. 7, the pressure inside the sealed packages has shown a slight increase (0.4 Torr) over the first 10 days, followed by no noticeable change.

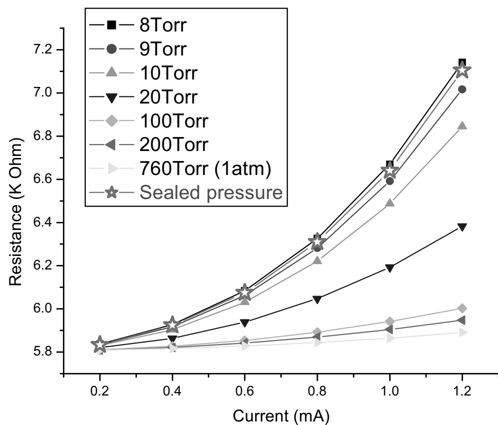

Figure 6: The resistance vs. current characteristics of a Pirani gauge. The pressure inside the sealed device (symbol "☆") is extracted to be around 8 Torr.

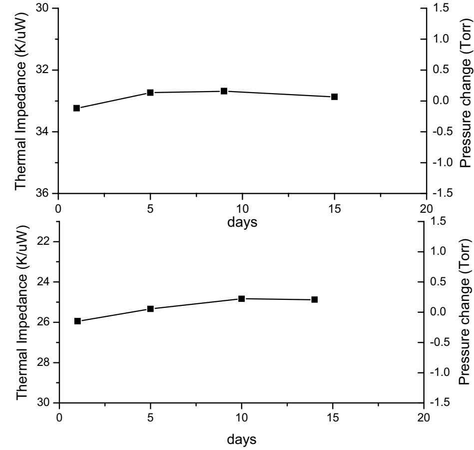

Figure 7: Leak rate of two sealed cavities.

The sealing material, which could have significant deposition inside the package if lithographically-defined etch holes in the encapsulation shell were to be sealed, was measured inside the sealed cavity in a separate test. The test sample has porous alumina cavities (1.5 µm thick) formed on a bare silicon substrate. After a 5000 Å PECVD oxide deposition was performed, the cavity was ruptured using a probe tip and the thickness of oxide on top of the silicon substrate inside the cavity was measured by Nanospec® using a thin oxide program (low limit: 20 Å). For all the samples tested, a "less than 20 Å" result was obtained, indicating the porous alumina shell effectively prevented the internal deposition of the sealing material during the sealing process.

4. RF PERFORMANCE

To investigate the RF performance of the porous alumina thin film package, a CPW (Coplanar Waveguide) line (Cr/Au: 250/8000 Å) was packaged on a silicon substrate with high resistivity (> 2000 Ω·cm). Following a similar process flow to the one in Fig. 4, the porous alumina cavity was formed by removing the Ti/Au seed layer and the a-Si sacrificial layer sequentially. A PECVD deposition of 1 µm low stress silicon nitride sealed the cavity. The final step was etching away all the films above Au in the electrical contact area.

An optical microscopic top view of the fabricated device is displayed in Fig. 8(a). The sealed cavity is seen in the middle of the picture, measuring 160 µm by 300 µm, a typical size of a RF switch device. The Au signal line encapsulated inside the sealed cavity is clearly visible through the transparent encapsulation shell, which is composed of 1.2 µm porous alumina and 1 µm silicon nitride thin films.

The insertion loss introduced by the package, extracted from the difference between red (packaged CPW) and black (un-packaged CPW) lines in Fig. 9, was less than 0.1 dB up to 40 GHz. This small amount of insertion loss is likely due to the silicon sacrificial layer left in the feed-through area (Fig. 8(b)). Removing the sacrificial layer in the feed-through by adding a lithography and etching step can further reduce the insertion loss of the package.

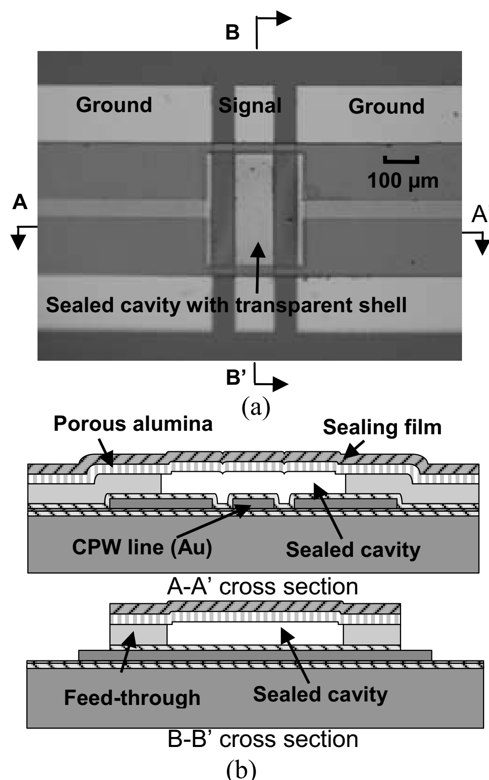

Figure 8: An encapsulated CPW device. The Au signal line is clearly visible through the transparent porous alumina shell in (a). Schematic cross section views are shown in (b).

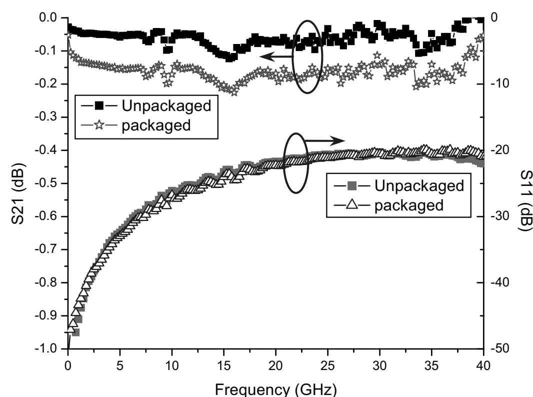

Figure 9: The insertion loss difference (left axis) – less than 0.1 dB up to 40 GHz – between packaged and unpackaged CPW device demonstrates the reported encapsulation has a very small influence on the performance of a RF device.

4. CONCLUSION

Porous alumina thin film, obtained by anodization etching on evaporated or sputter aluminum thin film at room temperature, was discovered to be an excellent choice as an encapsulation layer for low-temperature on-wafer thin-film packaging. A surface-micromachining process combined with anodization etching was developed to fabricate the free-standing porous alumina thin film membrane. A porous alumina thin film package was successfully fabricated to seal a free-standing metal microdevice in vacuum (8 Torr) and has demonstrated hermeticity for the initial one month (as of Sept. 30, 2005). The influence of the porous alumina thin-film package on the RF performance of MEMS devices was measured to be exceptionally low – less than 0.1 dB insertion loss up to 40 GHz.

5. ACKNOWLEDGEMENT

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6. REFERENCES

1. W.H. Ko, J.T. Suminto, and G.J. Yeh, *"Bonding techniques for microsensors"* in *Micromachining and Micropackaging of Transducers*, Elsevier, New York, 1985
2. K.E. Peterson and P. Barth, "Silicon fusion bonding for pressure sensors," *Proceedings of Solid State Sensor and Actuator Workshop*, Hilton Head, SC, pp. 144-147, 1988.
3. L. Lin, "MEMS post-packaging by localized heating and bonding," *Journal of Microelectromechanical Systems*, vol. 23, pp. 608 - 616, 2000.
4. R. He and C.-J. Kim, "On-chip hermetic packaging enabled by post-deposition electrochemical etching of polysilicon," *Proceedings of IEEE Conference on Micro Electro Mechanical Systems (MEMS'05)*, Miami, Florida, pp. 544-547, Jan., 2005.
5. B.H. Stark and K. Najafi, "A low-temperature thin-film electroplated metal vacuum package," *Journal of Microelectromechanical Systems*, vol. 13, pp. 147-157, 2004.
6. R.N. Candler, W.-T. Park, H. Li, G. Yama, A. Partridge, M. Lutz, and T.W. Kenny, "Single wafer encapsulation of MEMS devices," *IEEE Transactions on Advanced Packaging*, vol. 26, pp. 227-232, 2003.
7. R. Aigner, K.-G. Oppermann, H. Kapels, and S. Kolb, ""Cavity-micromachining" technology: zero-package solution for inertial sensors," *Proceedings of 11th International Conference on Solid-State Sensors and Actuators (Transducers'01)*, Munich, Germany, pp. 186-189, June 10-14, 2001.
8. K.S. Lebouitz, A. Mazaheri, R.T. Howe, and A.P. Pisano, "Vacuum encapsulation of resonant devices using permeable polysilicon," *Proceedings of IEEE Conference on Microelectromechanical Systems (MEMS'99)*, Orlando, FL, pp. 470-475, Jan., 1999.
9. T. Tsuchiya, Y. Kageyama, H. Funabashi, and J. Sakata, "Polysilicon vibrating gyroscope vacuum-encapsulated in an on-chip micro chamber," *Sensors and Actuators A: Physical*, vol. 90, pp. 49-55, 2001.
10. J.L. Lund, C.V. Jahnes, H. Deligianni, L.P. Buchwalter, J.M. Cotte, P. Andricacos, D.E. Seeger*, et al.*, "A Low Temperature Bi-CMOS Compatible Process for MEMS RF Resonators and Filters," *Proceedings of Solid-State Sensor, Actuator and Microsystems Workshop (Hilton Head'02)*, Hilton Head Island, South Carolina, pp. 38-42, June 2-6, 2002.
11. D.I. Forehand and C.L. Goldsmith, "Wafer Level Micropackaging for RF MEMS Switches," *2005 ASME InterPACK '05 Tech Conf*, San Francisco, CA, July, 2005.
12. R. He, L. Fan, M.C. Wu, and C.-J. Kim, "Porous Polysilicon Shell Formed by Electrochemical Etching for On-Chip Vacuum Encapsulation," *Proceedings of Solid-State Sensor, Actuator and Microsystems Workshop (HH'04)*, Hilton Head Island, South Carolina, pp. 332-5, June 6-10, 2004.
13. S.Z. Chu, K. Wada, S. Inoue, and S. Todoroki, "Formation and Microstructures of Anodic Alumina Films from Aluminum Sputtered on Glass Substrate," *Journal of The Electrochemical Society*, vol. 149, pp. B321-B327, 2002.